ELECTRONC CIRCUIT ANALYSIS LECTURE NOTES (R22A0408)

B.TECH (II YEAR – II SEM) (2023-24)

Prepared by:

DR. CHINNA RAO, Associate Professor

Mr. SHIVARAJ KUMAR, Assistant Professor

Department of Electronics and Communication Engineering

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

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Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

II Year B.Tech. ECE- II Sem

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(R22A0408) ELECTRONIC CIRCUIT ANALYSIS

Course Objectives:

Upon completing this course, the student twill be able to

1. Learn the concepts of Power Amplifiers.
2. To give understanding of tuned amplifier circuits
3. Understand various multivibrators using transistors and sweep circuits.

UNIT – I

Large Signal Amplifiers: Class A Power Amplifier- Series fed and Transformer coupled, Conversion Efficiency, Class B Power Amplifier- Push Pull and Complimentary Symmetry configurations, Conversion Efficiency, Principle of operation of Class AB and Class –C and D Amplifiers.

UNIT- II

Tuned Amplifiers: Introduction, single Tuned Amplifiers – Q-factor, frequency response, Double Tuned Amplifiers – Q-factor, frequency response, Concept of stagger tuning and synchronous tuning

UNIT - III

Multivibrators: Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using Transistors.

UNIT - IV

Time Base Generators: General features of a Time base Signal, Methods of Generating Time Base Waveform, concepts of Transistor Miller and Bootstrap Time Base Generator, Methods of Linearity improvement.

UNIT - V

Sampling Gates: Basic operating principles of Sampling Gates, Unidirectional and Bi-directional Sampling Gates, Four Diode Sampling Gate, Reduction of pedestal in Gate Circuits

Synchronization and Frequency Division: Pulse Synchronization of Relaxation Devices, Frequency division in Sweep Circuits, Stability of Relaxation Devices,

TEXT BOOKS:

1. Jacob Millman, Christos C Halkias - Integrated Electronics, , McGraw Hill Education.
2. J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms –2nd Ed., TMH, 2008,

REFERENCE BOOKS:

1. David A. Bell - Electronic Devices and Circuits, 5th Ed., Oxford.
2. Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
3. Ronald J. Tocci - Fundamentals of Pulse and Digital Circuits, 3rd Ed., 2008.
4. David A. Bell - Pulse, Switching and Digital Circuits, 5th Ed., Oxford, 2015.

Course Outcomes:

Upon completing this course, the student will be able to

1. Design the power amplifiers
2. Design the tuned amplifiers and analyse is frequency response
3. Design Multivibrators and sweep circuits for various applications.
4. Utilize the concepts of synchronization, frequency division and sampling gates

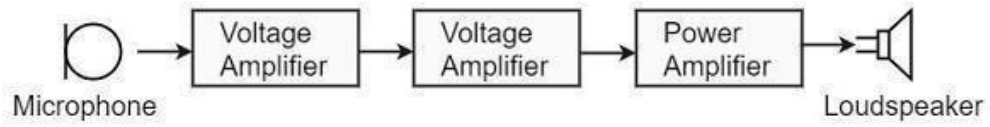
UNIT-I

LARGE SIGNAL AMPLIFIERS

In practice, any amplifier consists of few stages of amplification. If we consider audio amplification, it has several stages of amplification, depending upon our requirement.

Power Amplifier

After the audio signal is converted into electrical signal, it has several voltage amplifications done, after which the power amplification of the amplified signal is done just before the loud speaker stage. This is clearly shown in the below figure.



While the voltage amplifier raises the voltage level of the signal, the power amplifier raises the power level of the signal. Besides raising the power level, it can also be said that a power amplifier is a device which converts DC power to AC power and whose action is controlled by the input signal.

The DC power is distributed according to the relation, DC

power input = AC power output + losses

Power Transistor

For such Power amplification, a normal transistor would not do. A transistor that is manufactured to suit the purpose of power amplification is called as a **Power transistor**.

A Power transistor differs from the other transistors, in the following factors.

- It is larger in size, in order to handle large powers.
- The collector region of the transistor is made large and a heat sink is placed at the collector-base junction in order to minimize heat generated.
- The emitter and base regions of a power transistor are heavily doped.
- Due to the low input resistance, it requires low input power.

Hence there is a lot of difference in voltage amplification and power amplification. So, let us now try to get into the details to understand the differences between a voltage amplifier and a power amplifier.

Difference between Voltage and Power Amplifiers:

Let us try to differentiate between voltage and power amplifier.

Voltage Amplifier

The function of a voltage amplifier is to raise the voltage level of the signal. A voltage

amplifier is designed to achieve maximum voltage amplification.

The voltage gain of an amplifier is given by

$$Av=\beta(Rc/Rin)$$

The characteristics of a voltage amplifier are as follows −

- The base of the transistor should be thin and hence the value of β should be greater than 100.
- The resistance of the input resistor R_{in} should be low when compared to collector load R_C.
- The collector load R_C should be relatively high. To permit high collector load, the voltage amplifiers are always operated at low collector current.
- The voltage amplifiers are used for small signal voltages.

Power Amplifier

The function of a power amplifier is to raise the power level of input signal. It is required to deliver a large amount of power and has to handle large current.

The characteristics of a power amplifier are as follows –

- The base of transistor is made thicken to handle large currents. The value of β being (β > 100) high.
- The size of the transistor is made larger, in order to dissipate more heat, which is produced during transistor operation.
- Transformer coupling is used for impedance matching.
- Collector resistance is made low.

The comparison between voltage and power amplifiers is given below in a tabular form.

S.No	Particular	Voltage Amplifier	Power Amplifier
1	β	High (>100)	Low (5 to 20)
2	R_C	High (4-10 KΩ)	Low (5 to 20 Ω)
3	Coupling	Usually R-C coupling	Invariably transformer coupling
4	Input voltage	Low (a few m V)	High (2-4 V)
5	Collector current	Low (≈ 1 mA)	High (> 100 mA)
6	Power output	Low	High
7	Output impendence	High (≈ 12 K Ω)	Low (200 Ω

The Power amplifiers amplify the power level of the signal. This amplification is done in the last stage in audio applications. The applications related to radio frequencies employ radio power amplifiers. But the **operating point** of a transistor plays a very important role in determining the efficiency of the amplifier. The **main classification** is done based on this mode of operation.

The classification is done based on their frequencies and also based on their mode of operation.

Classification Based on Frequencies

Power amplifiers are divided into two categories, based on the frequencies they handle. They are as follows.

- **Audio Power Amplifiers** − The audio power amplifiers raise the power level of signals that have audio frequency range (20 Hz to 20 KHz). They are also known as **Small signal power amplifiers**.
- **Radio Power Amplifiers** − Radio Power Amplifiers or tuned power amplifiers raise the power level of signals that have radio frequency range (3 KHz to 300 GHz). They are also known as **large signal power amplifiers**.

Classification Based on Mode of Operation

On the basis of the mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as follows.

- **Class A Power amplifier** − When the collector current flows at all times during the full cycle of signal, the power amplifier is known as **class A poweramplifier**.
- **Class B Power amplifier** − When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.
- **Class C Power amplifier** − When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**.

There forms another amplifier called Class AB amplifier, if we combine the class A and class B amplifiers so as to utilize the advantages of both. Before going into the details of these amplifiers, let us have a look at the important terms that have to be considered to determine the efficiency of an amplifier.

Terms Considering Performance

The primary objective of a power amplifier is to obtain maximum output power. In order to

achieve this, the important factors to be considered are collector efficiency, power dissipation capability and distortion. Let us go through them in detail.

Collector Efficiency

This explains how well an amplifier converts DC power to AC power. When the DC supply is given by the battery but no AC signal input is given, the collector output at such a condition is observed as **collector efficiency**.

The collector efficiency is defined as

η=average a.c power output / average d.c power input to transistor

The main aim of a power amplifier is to obtain maximum collector efficiency. Hence the higher the value of collector efficiency, the efficient the amplifier will be.

Power Dissipation Capacity

Every transistor gets heated up during its operation. As a power transistor handles large currents, it gets more heated up. This heat increases the temperature of the transistor, which alters the operating point of the transistor. So, in order to maintain the operating point stability, the temperature of the transistor has to be kept in permissible limits. For this, the heat produced has to be dissipated. Such a capacity is called as Power dissipation capability.

Power dissipation capability can be defined as the ability of a power transistor to dissipate the heat developed in it. Metal cases called heat sinks are used in order to dissipate the heat produced in power transistors.

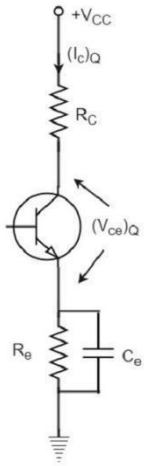
Distortion

A transistor is a non-linear device. When compared with the input, there occur few variations in the output. In voltage amplifiers, this problem is not pre-dominant as small currents are used. But in power amplifiers, as large currents are in use, the problem of distortion certainly arises.

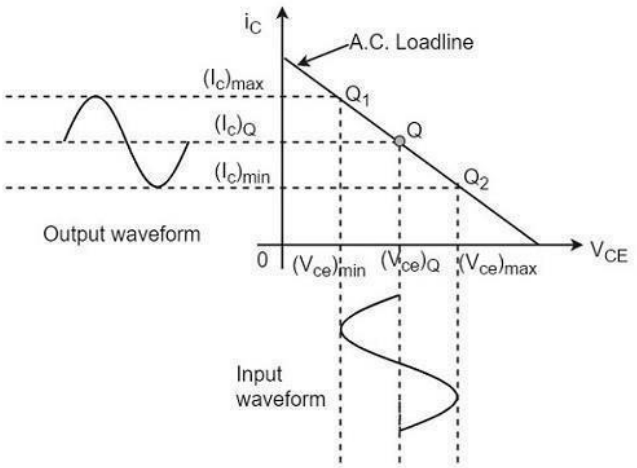
Distortion is defined as the change of output wave shape from the input wave shape of the amplifier. An amplifier that has lesser distortion produces a better output and hence considered efficient.

We have already come across the details of transistor biasing, which is very important for the operation of a transistor as an amplifier. Hence to achieve faithful amplification, the biasing of the transistor has to be done such that the amplifier operates over the linear region.

A Class A power amplifier is one in which the output current flows for the entire cycle of the AC input supply. Hence the complete signal present at the input is amplified at the output. The following figure shows the circuit diagram for Class A Power amplifier.



From the above figure, it can be observed that the transformer is present at the collector as a load. The use of transformer permits the impedance matching, resulting in the transference of maximum power to the load e.g. loud speaker.



The operating point of this amplifier is present in the linear region. It is so selected that the current flows for the entire ac input cycle. The below figure explains the selection of operating point.

The output characteristics with operating point Q is shown in the figure above. Here $(I_c)_Q$ and $(V_{ce})_Q$ represent no signal collector current and voltage between collector and emitter respectively. When signal is applied, the Q-point shifts to Q_1 and Q_2. The output current increases to $(I_c)_{max}$ and decreases to $(I_c)_{min}$. Similarly, the collector-emitter voltage increases to $(V_{ce})_{max}$ and decreases to $(V_{ce})_{min}$.

D.C. Power drawn from collector battery V_{cc} is given by

$$Pin=voltage\times current=V_{CC}(I_C)_Q$$

This power is used in the following two parts −

- Power dissipated in the collector load as heat is given by

$$P_{RC}=(current)^2\times resistance=(IC)^2{}_QR_C$$

- Power given to transistor is given by

$$P_{tr}=P_{in}-P_{RC}=V_{CC}-(I_C)_{2Q}R_C$$

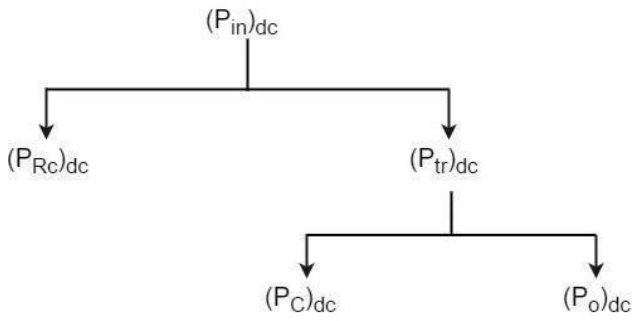
When signal is applied, the power given to transistor is used in the following two parts −

- A.C. Power developed across load resistors RC which constitutes the a.c. power output.

$$(P_O)ac=I^2R_C=V^2\,/\,R_C=(V_m/\sqrt{2}\,)\,/R_C=V2m/2R_C$$

- Where **I** is the R.M.S. value of a.c. output current through load, **V** is the R.M.S. value of a.c. voltage, and $\mathbf{V_m}$ is the maximum value of V.
- The D.C. power dissipated by the transistor (collector region) in the form of heat, i.e., $(P_C)_{dc}$

We have represented the whole power flow in the following diagram.



This class A power amplifier can amplify small signals with least distortion and the output will be an exact replica of the input with increased strength.

Let us now try to draw some expressions to represent efficiencies.

Overall Efficiency

The overall efficiency of the amplifier circuit is given by

$$(\eta)_{overall} = \frac{a.c power\ delivered to the\ load}{total\ power\ delivered by\ d.c\ supply}$$

$$= \frac{(P_O)_{ac}}{(P_{in})_{dc}}$$

Collector Efficiency

The collector efficiency of the transistor is defined as

$$(\eta)_{collector} = \frac{average\ a.c power\ output}{average\ d.c power\ input to transistor}$$

$$= \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Expression for overall efficiency

$$(P_O)_{ac} = V_{rms} \times I_{rms}$$

$$= \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] \times \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right]$$

$$= \frac{[(V_{ce})_{max} - (V_{ce})_{min}] \times [(I_C)_{max} - (I_C)_{min}]}{8}$$

Advantages of Class A Amplifiers

The advantages of Class A power amplifier are as follows −

- The current flows for complete input cycle
- It can amplify small signals
- The output is same as input
- No distortion is present

Disadvantages of Class A Amplifiers

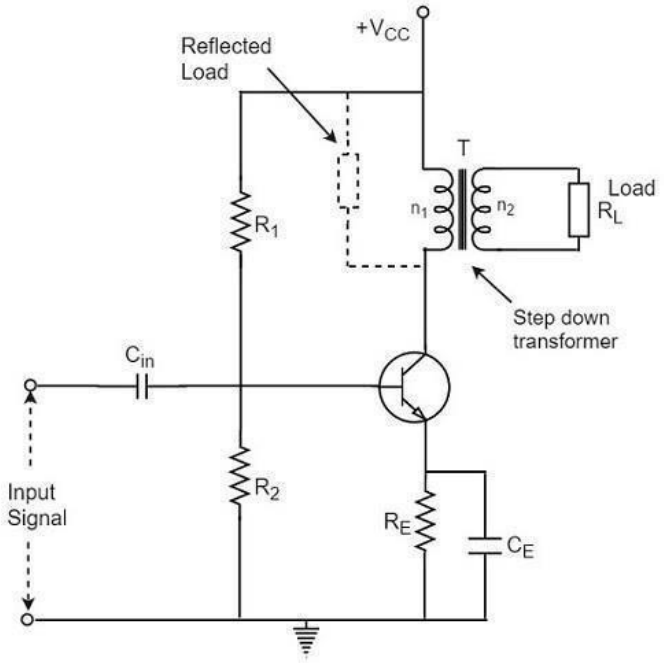
The advantages of Class A power amplifier are as follows −

- Low power output
- Low collector efficiency

The class A power amplifier as discussed in the previous chapter, is the circuit in which the output current flows for the entire cycle of the AC input supply. We also have learnt about the

disadvantages it has such as low output power and efficiency. In order to minimize those effects, the transformer coupled class A power amplifier has been introduced.

The **construction of class A power amplifier** can be understood with the help of below figure. This is similar to the normal amplifier circuit but connected with a transformer in the collector load.

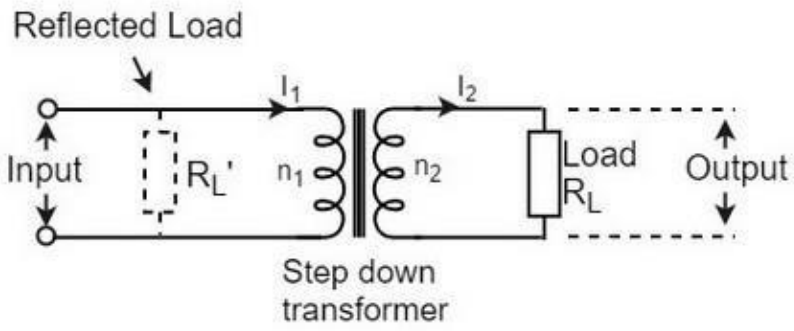


Here R_1 and R_2 provide potential divider arrangement. The resistor Re provides stabilization, C_e is the bypass capacitor and R_e to prevent a.c. voltage. The transformer used here is a step-down transformer.The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

Transformer Action:

The transformer used in the collector circuit is for impedance matching. R_L is the load connected in the secondary of a transformer. R_L' is the reflected load in the primary of the transformer.

The number of turns in the primary are n_1 and the secondary are n_2. Let V_1 and V_2 be the primary and secondary voltages and I_1 and I_2 be the primary and secondary currents respectively. The below figure shows the transformer clearly.



We know that

$$\frac{V_1}{V_2} = \frac{n_1}{n_2} \; and \; \frac{I_1}{I_2} = \frac{n_1}{n_2}$$

Or

$$V_1 = \frac{n_1}{n_2} V_2 \; and \; I_1 = \frac{n_1}{n_2} I_2$$

Hence

$$\frac{V_1}{I_1} = \left(\frac{n_1}{n_2}\right)^2 \frac{V_2}{I_2}$$

But $V_1/I_1 = R_L'$ = effective input resistance

And $V_2/I_2 = R_L$ = effective output resistance

Therefore,

$$R_L' = \left(\frac{n_1}{n_2}\right)^2 R_L = n^2 R_L$$

Where

$$n = \frac{number \; of \; turns \; in \; primary}{number \; of \; turns \; in \; secondary} = \frac{n_1}{n_2}$$

A power amplifier may be matched by taking proper turn ratio in step down transformer.

Circuit Operation

If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line.

The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector voltage appears across the primary of the transformer.

Circuit Analysis

The power loss in the primary is assumed to be negligible, as its resistance is very small.

The input power under dc condition will be

$$(P_{in})_{dc} = (P_{tr})_{dc} = V_{CC} \times (I_C)_Q$$

Under maximum capacity of class A amplifier, voltage swings from $(V_{ce})_{max}$ to zero and current from $(I_C)_{max}$ to zero.

Hence

$$V_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max}}{2}\right] = \frac{2V_{CC}}{2\sqrt{2}}$$

$$= \frac{V_{CC}}{\sqrt{2}}$$

$$I_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max}}{2}\right] = \frac{2(I_C)_Q}{2\sqrt{2}}$$

$$= \frac{(I_C)_Q}{\sqrt{2}}$$

Therefore,

$$(P_O)_{ac} = V_{rms} \times I_{rms} = \frac{V_{CC}}{\sqrt{2}} \times \frac{(I_C)_Q}{\sqrt{2}} = \frac{V_{CC} \times (I_C)_Q}{2}$$

Therefore,

$$\text{Collector Efficiency} = \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Or,

$$(\eta)_{collector} = \frac{V_{CC} \times (I_C)_Q}{2 \times V_{CC} \times (I_C)_Q} = \frac{1}{2}$$

$$= \frac{1}{2} \times 100 = 50\%$$

The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

Advantages

The advantages of transformer coupled class A power amplifier are as follows.

- No loss of signal power in the base or collector resistors.
- Excellent impedance matching is achieved.
- Gain is high.
- DC isolation is provided.

Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows.

- Low frequency signals are less amplified comparatively.

- Hum noise is introduced by transformers.
- Transformers are bulky and costly.
- Poor frequency response.

Applications

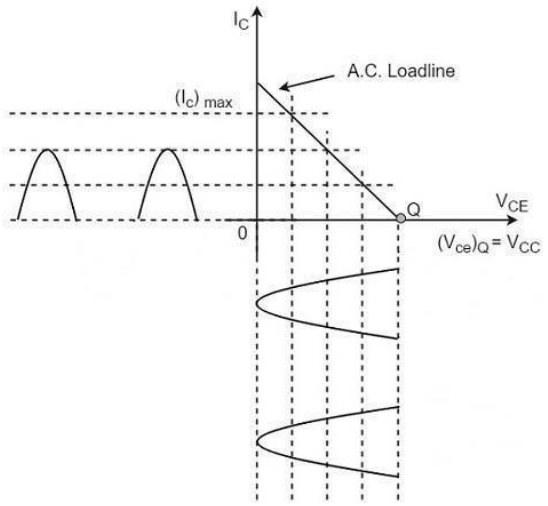
The applications of transformer coupled class A power amplifier are as follows.

- This circuit is where impedance matching is the main criterion.
- These are used as driver amplifiers and sometimes as output amplifiers.
- When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.

Class B Operation

The biasing of the transistor in class B operation is in such a way that at zero signal condition, there will be no collector current. The **operating point** is selected to be at collector cut off voltage. So, when the signal is applied, **only the positive half cycle** is amplified at the output.

The figure below shows the input and output waveforms during class B operation.



When the signal is applied, the circuit is forward biased for the positive half cycle of the input and hence the collector current flows. But during the negative half cycle of the input, the circuit is reverse biased and the collector current will be absent. Hence **only the positive half cycle** is amplified at the output.

As the negative half cycle is completely absent, the signal distortion will be high. Also, when the applied signal increases, the power dissipation will be more. But when compared to class A power amplifier, the output efficiency is increased. Well, in order to minimize the disadvantages and achieve low distortion, high efficiency and high output power, the push-pull configuration is used in this class B amplifier.

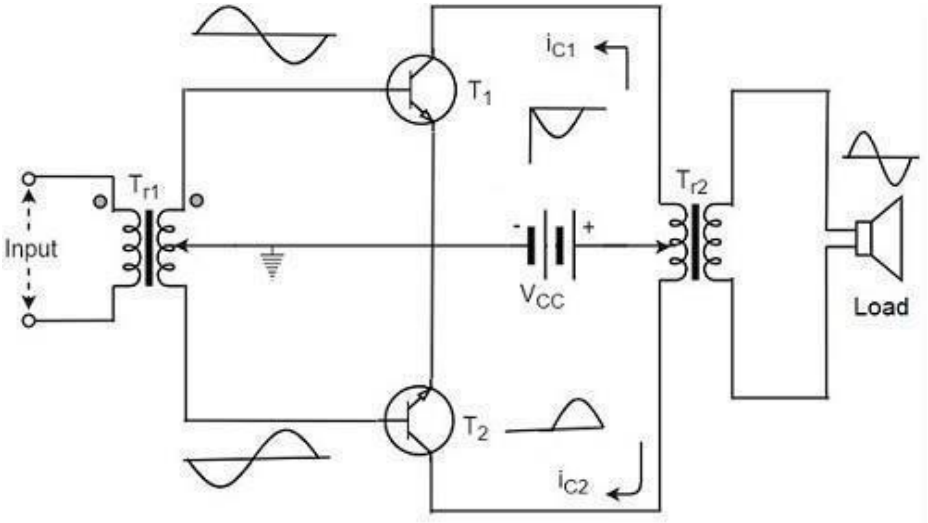
Class B Push-Pull Amplifier

Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

Construction:

The circuit of a push-pull class B power amplifier consists of two identical transistors T_1 and T_2 whose bases are connected to the secondary of the center-tapped input transformer T_{r1}. The emitters are shorted and the collectors are given the V_{CC} supply through the primary of the output transformer T_{r2}.

The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.

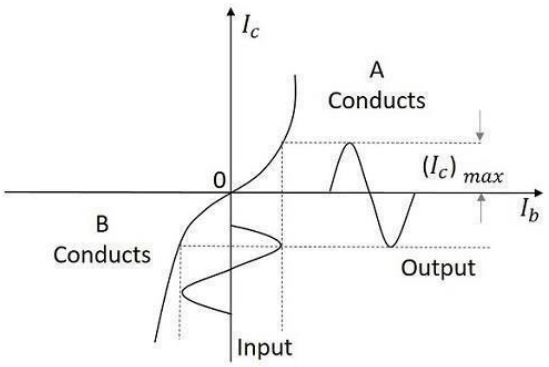


The circuit operation of class B push pull amplifier is detailed below.

Operation

The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T_1 and T_2 are in cut off condition and hence no collector currents flow. As no current is drawn from V_{CC}, no power is wasted.

When input signal is given, it is applied to the input transformer T_{r1} which splits the signal into two signals that are 180^o out of phase with each other. These two signals are given to the two identical transistors T_1 and T_2. For the positive half cycle, the base of the transistor T_1 becomes positive and collector current flows. At the same time, the transistor T_2 has negative half cycle, which throws the transistor T_2 into cutoff condition and hence no collector current flows. The waveform is produced as shown in the following figure.



For the next half cycle, the transistor T_1 gets into cut off condition and the transistor T_2 gets into conduction, to contribute the output. Hence for both the cycles, each transistor conducts alternately. The output transformer T_{r3} serves to join the two currents producing an almost undistorted output waveform.

Power Efficiency of Class B Push-Pull Amplifier

The current in each transistor is the average value of half sine loop. For half sine loop, I_{dc} is given by $I_{dc} = \frac{(I_C)_{max}}{\pi}$

Therefore,

$$(p_{in})_{dc} = 2 \times \left[\frac{(I_C)_{max}}{\pi} \times V_{CC}\right]$$

Here factor 2 is introduced as there are two transistors in push-pull amplifier.

R.M.S. value of collector current = $(I_C)_{max}/\sqrt{2}$

R.M.S. value of output voltage = $V_{CC}/\sqrt{2}$

Under ideal conditions of maximum power

Therefore,

$$(P_O)_{ac} = \frac{(I_C)_{max}}{\sqrt{2}} \times \frac{V_{CC}}{\sqrt{2}} = \frac{(I_C)_{max} \times V_{CC}}{2}$$

Now overall maximum efficiency

$$\eta_{overall} = \frac{(P_O)_{ac}}{(P_{in})_{dc}}$$

$$= \frac{(I_C)_{max} \times V_{CC}}{2} \times \frac{\pi}{2(I_C)_{max} \times V_{CC}}$$

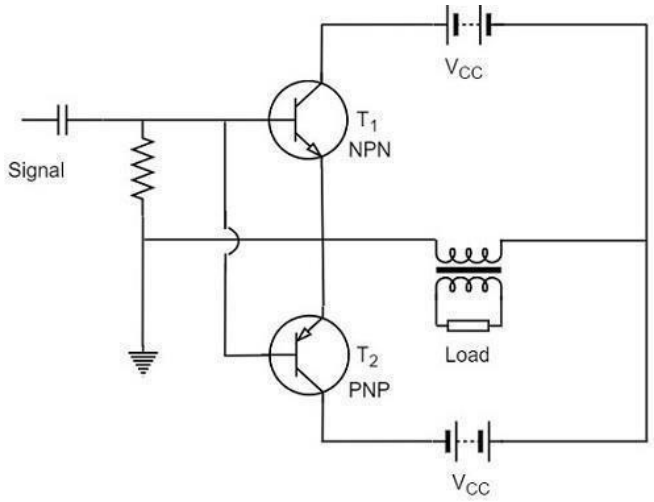
$$= \frac{\pi}{4} = 0.785 = 78.5\%$$

The collector efficiency would be the same.

Hence the class B push-pull amplifier improves the efficiency than the class A push-pull amplifier.

Complementary Symmetry Push-Pull Class B Amplifier

The push pull amplifier which was just discussed improves efficiency but the usage of center-tapped transformers makes the circuit bulky, heavy and costly. To make the circuit simple and to improve the efficiency, the transistors used can be complemented, as shown in the following circuit diagram.



The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts.

In this way, the NPN transistor amplifies during positive half cycle of the input, while PNP transistor amplifies during negative half cycle of the input. As the transistors are both complement to each other, yet act symmetrically while being connected in push pull configuration of class B, this circuit is termed as **Complementary symmetry push pull class B amplifier**.

Advantages

The advantages of Complementary symmetry push pull class B amplifier are as follows.

- As there is no need of center tapped transformers, the weight and cost are reduced.
- Equal and opposite input signal voltages are not required.

Disadvantages

The disadvantages of Complementary symmetry push pull class B amplifier are as follows.

- It is difficult to get a pair of transistors (NPN and PNP) that have similar characteristics.
- We require both positive and negative supply voltages.

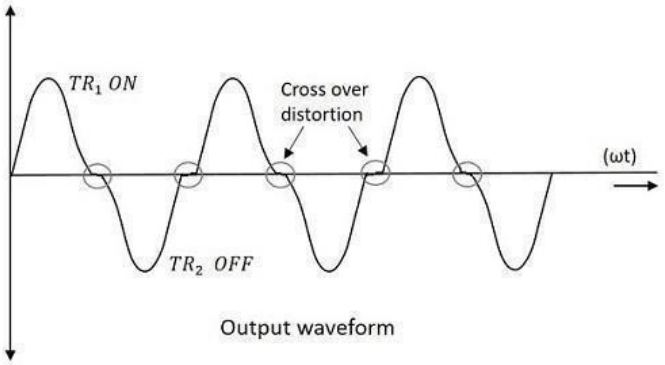
The class A and class B amplifier so far discussed has got few limitations. Let us now try to combine these two to get a new circuit which would have all the advantages of both class A and class B amplifier without their inefficiencies. Before that, let us also go through another important problem, called as **Cross over distortion**, the output of class B encounters with.

Cross-over Distortion:

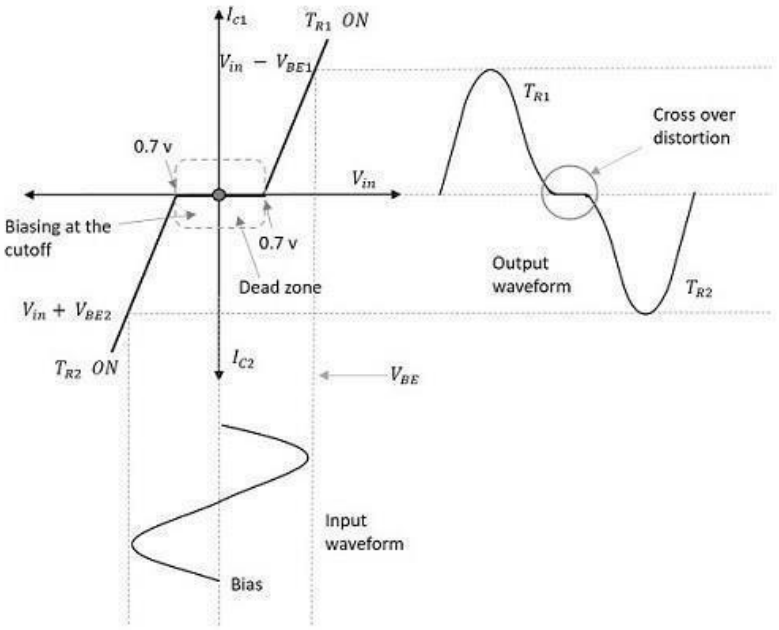
In the push-pull configuration, the two identical transistors get into conduction, one after the other and the output produced will be the combination of both.

When the signal changes or crosses over from one transistor to the other at the zero voltage point, it produces an amount of distortion to the output wave shape. For a transistor in order to conduct, the base emitter junction should cross 0.7v, the cut off voltage. The time taken for a transistor to get ON from OFF or to get OFF from ON state is called the **transition period**.

At the zero voltage point, the transition period of switching over the transistors from one to the other, has its effect which leads to the instances where both the transistors are OFF at a time. Such instances can be called as **Flat spot** or **Dead band** on the output wave shape.



The above figure clearly shows the cross over distortion which is prominent in the output waveform. This is the main disadvantage. This cross over distortion effect also reduces the overall peak to peak value of the output waveform which in turn reduces the maximum power output. This can be more clearly understood through the non-linear characteristic of the waveform as shown below.



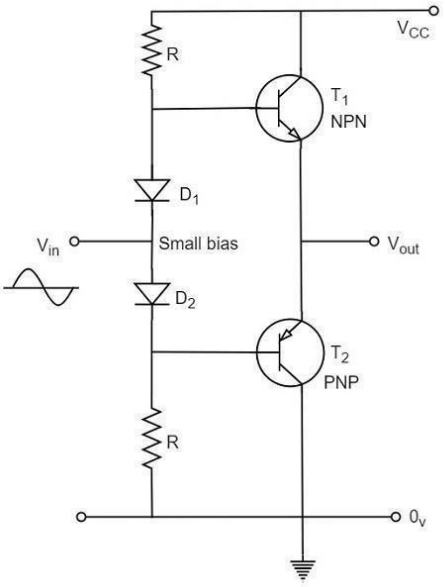
It is understood that this cross-over distortion is less pronounced for large input signals, where as it causes severe disturbance for small input signals. This cross over distortion can be eliminated if the conduction of the amplifier is more than one half cycle, so that both the transistors won't be OFF at the same time.

This idea leads to the invention of class AB amplifier, which is the combination of both class A and class B amplifiers, as discussed below.

Class AB Power Amplifier

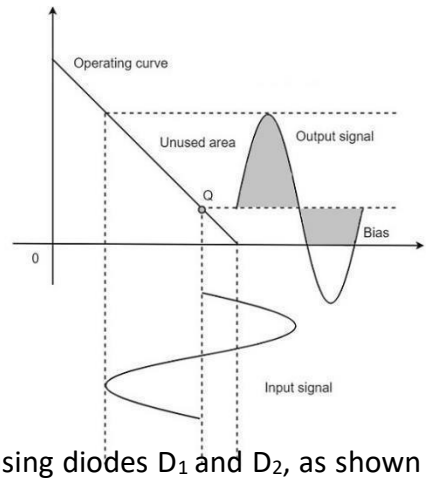
As the name implies, class AB is a combination of class A and class B type of amplifiers. As class A has the problem of low efficiency and class B has distortion problem, this class AB is emerged to eliminate these two problems, by utilizing the advantages of both the classes.

The cross over distortion is the problem that occurs when both the transistors are OFF at the same instant, during the transition period. In order to eliminate this, the condition has to be chosen for more than one half cycle. Hence, the other transistor gets into conduction, before the operating transistor switches to cut off state. This is achieved only by using class AB configuration, as shown in the following circuit diagram.



Therefore, in class AB amplifier design, each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

The conduction angle of class AB amplifier is somewhere between 180° to 360° depending upon the operating point selected. This is understood with the help of below figure.



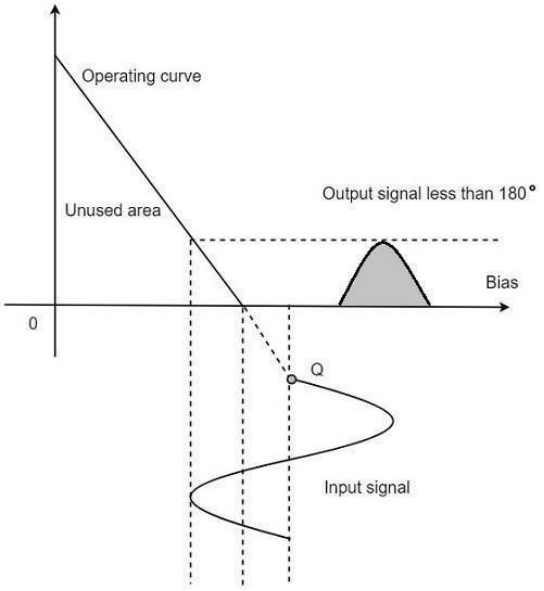
The small bias voltage given using diodes D_1 and D_2, as shown in the above figure, helps the operating point to be above the cutoff point. Hence the output waveform of class AB results as seen in the above figure. The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don't affect the circuit.

So, the class AB is a good compromise between class A and class B in terms of efficiency and linearity having the efficiency reaching about 50% to 60%. The class A, B and AB amplifiers are called as **linear amplifiers** because the output signal amplitude and phase are linearly related to the input signal amplitude and phase.

Class C Power Amplifier

When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**. The efficiency of class C amplifier is high while linearity is poor. The conduction angle for class C is less than 180°. It is generally around 90°, which means the transistor remains idle for more than half of the input signal. So, the output current will be delivered for less time compared to the application of input signal.

The following figure shows the operating point and output of a class C amplifier.



This kind of biasing gives a much improved efficiency of around 80% to the amplifier, but introduces heavy distortion in the output signal. Using the class C amplifier, the pulses produced at its output can be converted to complete sine wave of a particular frequency by using LC circuits in its collector circuit.

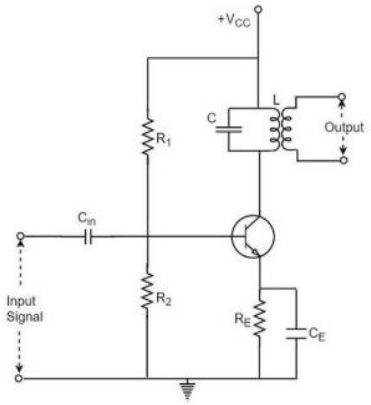
The types of amplifiers that we have discussed so far cannot work effectively at radio frequencies, even though they are good at audio frequencies. Also, the gain of these amplifiers is such that it will not vary according to the frequency of the signal, over a wide range. This allows the amplification of the signal equally well over a range of frequencies and does not permit the selection of particular desired frequency while rejecting the other frequencies.

UNIT-II

TUNED AMPLIFIERS

Tuned amplifiers are the amplifiers that are employed for the purpose of **tuning**. Tuning means selecting. Among a set of frequencies available, if there occurs a need to select a particular frequency, while rejecting all other frequencies, such a process is called **Selection**. This selection is done by using a circuit called as **Tuned circuit**.

When an amplifier circuit has its load replaced by a tuned circuit, such an amplifier can be called as a **Tuned amplifier circuit**. The basic tuned amplifier circuit looks as shown below.



The tuner circuit is nothing but a LC circuit which is also called as **resonant** or **tank circuit**. It selects the frequency. A tuned circuit is capable of amplifying a signal over a narrow band of frequencies that are centered at resonant frequency.

When the reactance of the inductor balances the reactance of the capacitor, in the tuned circuit at some frequency, such a frequency can be called as **resonant frequency**. It is denoted by $\mathbf{f_r}$.

The formula for resonance is

Types of Tuned Circuits

A tuned circuit can be Series tuned circuit (Series resonant circuit) or Parallel tuned circuit (parallel resonant circuit) according to the type of its connection to the main circuit.

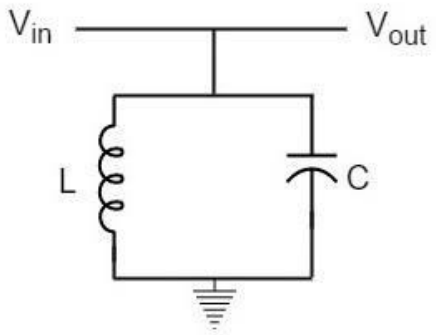
Series Tuned Circuit

The inductor and capacitor connected in series make a series tuned circuit, as shown in the following circuit diagram.

At resonant frequency, a series resonant circuit offers low impedance which allows high current through it. A series resonant circuit offers increasingly high impedance to the frequencies far from the resonant frequency.

Parallel Tuned Circuit

The inductor and capacitor connected in parallel make a parallel tuned circuit, as shown in the below figure.



At resonant frequency, a parallel resonant circuit offers high impedance which does not allow high current through it. A parallel resonant circuit offers increasingly low impedance to the frequencies far from the resonant frequency.

Characteristics of a Parallel Tuned Circuit

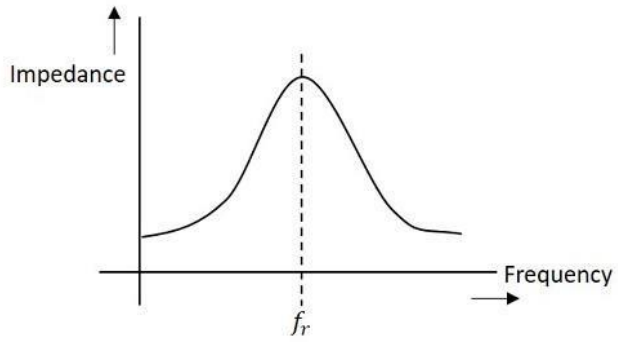
The frequency at which parallel resonance occurs (i.e. reactive component of circuit current becomes zero) is called the resonant frequency $\mathbf{f_r}$. The main characteristics of a tuned circuit are as follows.

Impedance

The ratio of supply voltage to the line current is the impedance of the tuned circuit. Impedance offered by LC circuit is given by

Supply voltage / Lineequation=V / I

At resonance, the line current increases while the impedance decreases.
The below figure represents the impedance curve of a parallel resonance circuit.



Impedance of the circuit decreases for the values above and below the resonant frequency $\mathbf{f_r}$. Hence the selection of a particular frequency and rejection of other frequencies is possible.

To obtain an equation for the circuit impedance, let us consider

Line Current $I=ILcos$□

$V/Zr=V/Z_L \times R/Z_L$

$1/Zr=R/Z^2_L$

$1/Zr=CR/L$

Since, $Z_{2L}=L/C$

Therefore, circuit impedance Z_r is obtained as

$Z_R=L/CR$

Thus at parallel resonance, the circuit impedance is equal to L/CR.

Circuit Current

At parallel resonance, the circuit or line current I is given by the applied voltage divided by the circuit impedance Z_r i.e.,

Line Current $I=VZr$

Where $Zr=L/CR$

Because Z_r is very high, the line current I will be very small.

Quality Factor

For a parallel resonance circuit, the sharpness of the resonance curve determines the selectivity. The smaller the resistance of the coil, the sharper the resonant curve will be. Hence the inductive reactance and resistance of the coil determine the quality of the tuned circuit.

The ratio of inductive reactance of the coil at resonance to its resistance is known as **Quality factor**. It is denoted by **Q**.

$Q=X_L/R=2\pi frLR$

The higher the value of Q, the sharper the resonance curve and the better the selectivity will be.

Advantages of Tuned Amplifiers

The following are the advantages of tuned amplifiers.

- The usage of reactive components like L and C, minimizes the power loss, which makes the tuned amplifiers efficient.
- The selectivity and amplification of desired frequency is high, by providing higher impedance at resonant frequency.
- A smaller collector supply VCC would do, because of its little resistance in parallel tuned circuit.

It is important to remember that these advantages are not applicable when there is a high resistive collector load.

Frequency Response of Tuned Amplifier

For an amplifier to be efficient, its gain should be high. This voltage gain depends upon β, input impedance and collector load. The collector load in a tuned amplifier is a tuned circuit.

The voltage gain of such an amplifier is given by

Voltage gain = Bz_c/Z_{in}

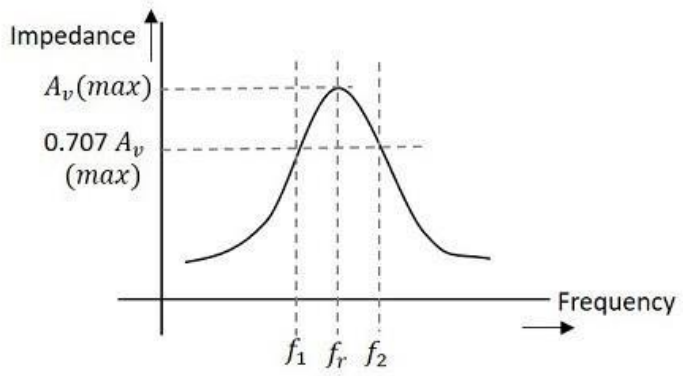
Where Z_C = effective collector load and Z_{in} = input impedance of the amplifier.

The value of Z_C depends upon the frequency of the tuned amplifier. As Z_C is maximum at resonant frequency, the gain of the amplifier is maximum at this resonant frequency.

Bandwidth

The range of frequencies at which the voltage gain of the tuned amplifier falls to 70.7% of the maximum gain is called its **Bandwidth**. The range of frequencies between f_1 and f_2 is called as bandwidth of the tuned amplifier. The bandwidth of a tuned amplifier depends upon the Q of the LC circuit i.e., upon the sharpness of the frequency response. The value of Q and the bandwidth are inversely proportional.

The figure below details the bandwidth and frequency response of the tuned amplifier.



Relation between Q and Bandwidth

The quality factor Q of the bandwidth is defined as the ratio of resonant frequency to bandwidth, i.e.,

Q=fr / BW

In general, a practical circuit has its Q value greater than 10.
Under this condition, the resonant frequency at parallel resonance is given by
$fr=1/\sqrt{2\pi LC}$
There are two main types of tuned amplifiers. They are −

- Single tuned amplifier
- Double tuned amplifier

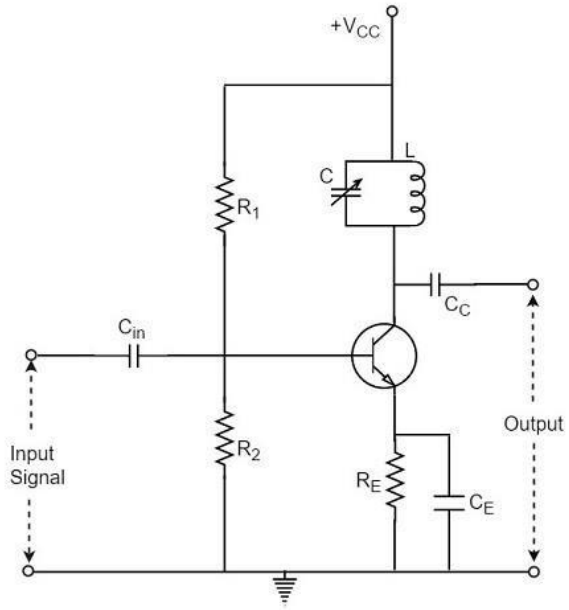
Single Tuned Amplifier

An amplifier circuit with a single tuner section being at the collector of the amplifier circuit is called as Single tuner amplifier circuit.

Construction

A simple transistor amplifier circuit consisting of a parallel tuned circuit in its collector load, makes a single tuned amplifier circuit. The values of capacitance and inductance of the tuned circuit are selected such that its resonant frequency is equal to the frequency to be amplified.

The following circuit diagram shows a single tuned amplifier circuit.



The output can be obtained from the coupling capacitor C_C as shown above or from a secondary winding placed at L.

Operation

The high frequency signal that has to be amplified is applied at the input of the amplifier. The resonant frequency of the parallel tuned circuit is made equal to the frequency of the signal applied by altering the capacitance value of the capacitor C, in the tuned circuit.At this stage, the tuned circuit offers high impedance to the signal frequency, which helps to offer high output across the tuned circuit. As high impedance is offered only for the tuned frequency, all the other frequencies which get lower impedance are rejected

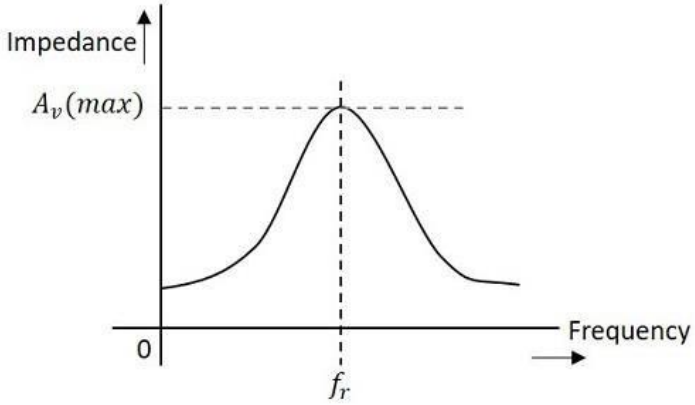
by the tuned circuit. Hence the tuned amplifier selects and amplifies the desired frequency signal.

Frequency Response

The parallel resonance occurs at resonant frequency f_r when the circuit has a high Q. the resonant frequency f_r is given by

$fr=1/\sqrt{2\pi LC}$

The following graph shows the frequency response of a single tuned amplifier circuit.



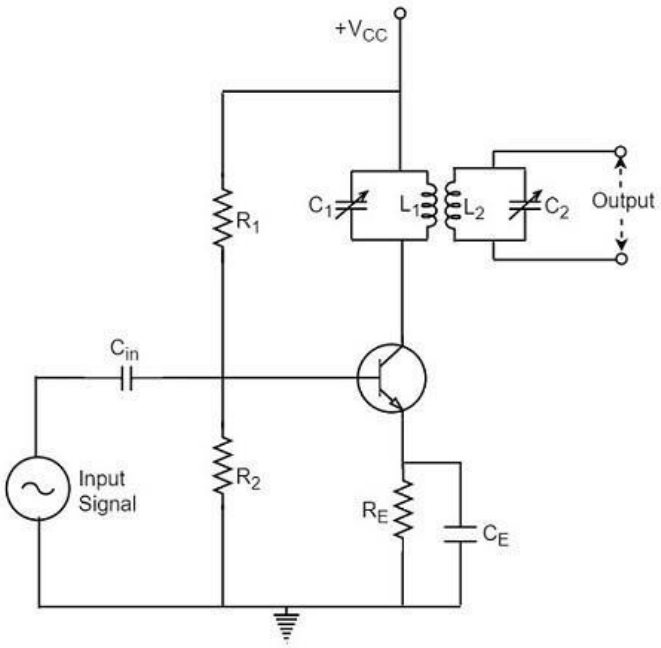
At resonant frequency f_r the impedance of parallel tuned circuit is very high and is purely resistive. The voltage across R_L is therefore maximum, when the circuit is tuned to resonant frequency. Hence the voltage gain is maximum at resonant frequency and drops off above and below it. The higher the Q, the narrower will the curve be.

Double Tuned Amplifier

An amplifier circuit with a double tuner section being at the collector of the amplifier circuit is called as Double tuner amplifier circuit.

Construction

The construction of double tuned amplifier is understood by having a look at the following figure. This circuit consists of two tuned circuits L_1C_1 and L_2C_2 in the collector section of the amplifier. The signal at the output of the tuned circuit L_1C_1 is coupled to the other tuned circuit L_2C_2 through mutual coupling method. The remaining circuit details are same as in the single tuned amplifier circuit, as shown in the following circuit diagram.



Operation

The high frequency signal which has to be amplified is given to the input of the amplifier. The tuning circuit L_1C_1 is tuned to the input signal frequency. At this condition, the tuned circuit offers high reactance to the signal frequency. Consequently, large output appears at the output of the tuned circuit L_1C_1 which is then coupled to the other tuned circuit L_2C_2 through mutual induction. These double tuned circuits are extensively used for coupling various circuits of radio and television receivers.

Frequency Response of Double Tuned Amplifier

The double tuned amplifier has the special feature of **coupling** which is important in determining the frequency response of the amplifier. The amount of mutual inductance between the two tuned circuits states the degree of coupling, which determines the frequency response of the circuit.

In order to have an idea on the mutual inductance property, let us go through the basic principle.

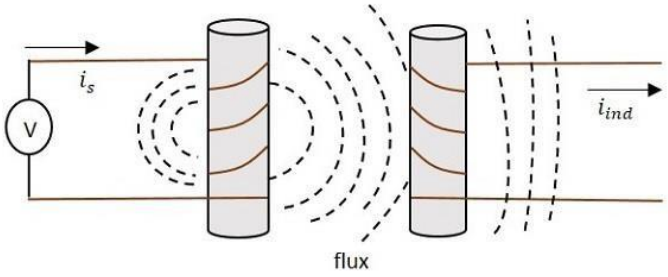
Mutual Inductance

As the current carrying coil produces some magnetic field around it, if another coil is brought near this coil, such that it is in the magnetic flux region of the primary, then the varying magnetic flux induces an EMF in the second coil. If this first coil is called as **Primary coil**, the second one can be called as a **Secondary coil**. When the EMF is induced in the secondary coil due to the varying magnetic field of the primary coil, then such phenomenon is called as the

.

Mutual Inductance.

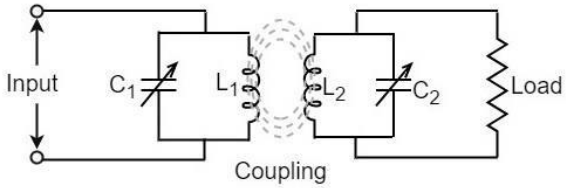
The figure below gives an idea about this.



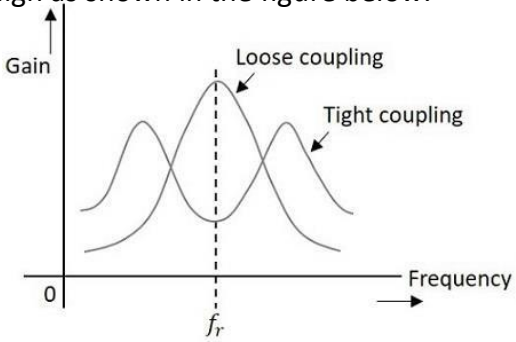
The current $\mathbf{i_s}$ in the figure indicate the source current while $\mathbf{i_{ind}}$ indicates the induced current. The flux represents the magnetic flux created around the coil. This spreads to the secondary coil also. With the application of voltage, the current $\mathbf{i_s}$ flows and flux gets created. When the current is varies the flux gets varied, producing $\mathbf{i_{ind}}$ in the secondary coil, due to the Mutual inductance property.

Coupling

Under the concept of mutual inductance coupling will be as shown in the figure below.



When the coils are spaced apart, the flux linkages of primary coil L_1 will not link the secondary coil L_2. At this condition, the coils are said to have **Loose coupling**. The resistance reflected from the secondary coil at this condition is small and the resonance curve will be sharp and the circuit Q is high as shown in the figure below.



UNIT III
MULTIVIBRATORS

A transistor can be used as a switch. It has three regions of operation. When both Emitter-to-base and collector-base junctions are reverse biased, the transistor operates in the cut-off region and it acts as an open switch. When the emitter base junction is forward biased and the Collector base junction is reverse biased, it operates in the active region and acts as auf amplifier. When both the emitter-base and collector-base junctions are forward biased, it Operates in the saturation region and acts as a closed switch. When the transistor is switched! from cut-off to saturation and from saturation to cut-off with negligible active region, the transistor is operated as a switch. When the transistor is in saturation, junction voltages are'i very small but the operating currents are large. When the transistor is in cut-off, the currents* are zero (except small leakage current) but the junction voltages are large.

In Below Figure the transistor Q can be used to connect and disconnect the load *RL* from the source Vcc When Q is saturated it is like a closed switch from collector to emitter and when Q is cutoff it is like an open switch from collector to emitter.

Referring to the output characteristics shown in Figure (b), the region below the IB = 0 curve is the cut-off region. The intersection of the load line with IB = 0 curve is the cut-off point. At this point, the base current is zero and the collector current is negligible. The emitter diode comes out of forward bias and the normal transistor action is lost, i.e, VCE(cut-off) = *Vcc.* The transistor appears like an open switch.

The intersection of the load line with the IB = IB(sat) curve is called the saturation point. At this point, the base current is IB(sat) and the collector current is maximum. 'At saturation, the collector diode comes out of cut-off and again the normal transistor action is lost, i.e. Ic(sat) = *Vcc / R_L* . IB(sat) represents the minimum base current required to bring the transistor into saturation. For 0 < IB < IB(sat), the transistor operates in the active region. If the base current is greater than IB(sat), the collector current approximately equals Vcc / RL and the transistor appears like a closed switch.

TRANSISTOR SWITCHING TIMES

When the transistor acts as a switch, it is either in cut-off or in saturation. To consider the behaviour of the transistor as it makes transition from one state to the other, consider the circuit shown in below figure (a) driven by the pulse waveform shown in Figure (b). The pulse waveform makes transitions between the voltage levels V2 and V1. At V2 the transistor is at cutoff and at V the transistor is in saturation. The input waveform v; is applied between the base and the emitter through a resistor *RB.*

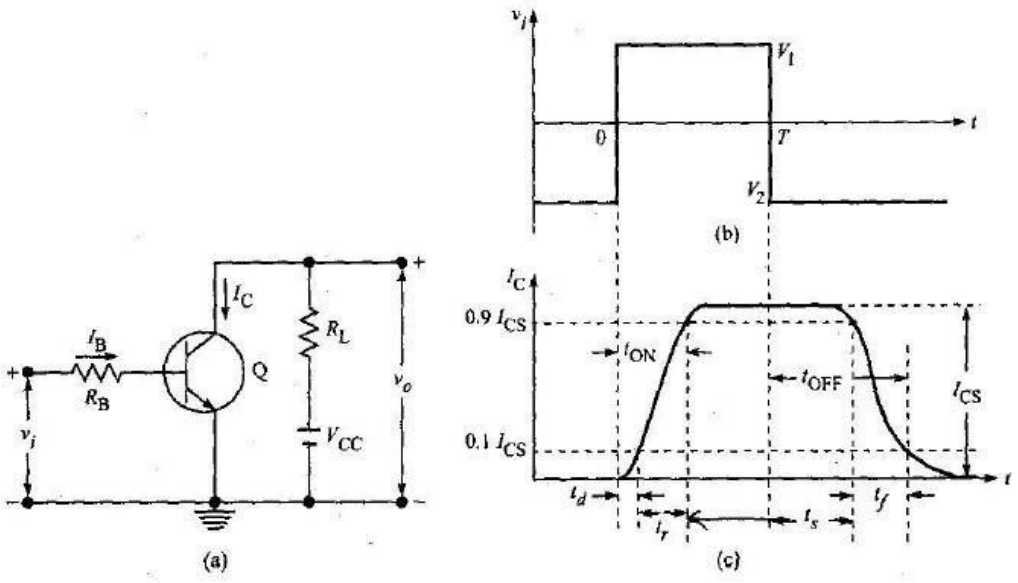


Figure a) Transistor as a Switch b) input waveform c) the response of collector current versus time

The response of the collector current ic to the input waveform, together with its time relationship to the waveform is shown in Figure (c), The collector current does not immediately respond to the input signal. Instead there is a delay, and the time that elapses during this delay, together with the time required for the current to rise to 10% of its maximum (saturation) value (Ics = Vcc / RL)) is called the delay time *td.* The current waveform has a nonzero rise time t r, which

is the rise time required for the current to rise from 10% to 90% of Ics- The total turn-on time TON is the sum of the *delay time* and the rise time, i.e. TON = *td + tr.*

When the input signal returns to its initial state, the collector current again fails to respond immediately. The interval which elapses between the transition of the input waveform and the time when Ic has dropped to 90% of Ics is called the *storage time ts.* The storage interval is followed by the fall time ly, which is the time required for 7C to fall from 90% to 10% of Ics- The turn-off time tOFF is defined as the sum of the storage and fall times, i.e. TOFF = *tr + tf* We shall now consider the physical reasons for the existence of each of these times.

The delay time

There are three factors that contribute to the delay time. First there is a delay which results from the fact that, when the driving signal is applied to the transistor input, a non-zero time is required to charge up the junction capacitance so that the transistor may be brought, from cut-off to the active region. Second, even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a nonzero time is required before these carriers can cross the base region to the collector junction and be recorded as collector current. Finally, a nonzero time is required before the collector current can rise to 10% of its maximum value. Rise time and fall time. The rise time and fall time are due to the fact that, if a base current step is used to saturate the transistor or to return it from saturation into cutoff, the collector current must traverse the active region. The collector current increases or decreases along an exponential curve. Storage time The failure of the transistor to respond to the trailing edge of the driving pulse for the time interval *ts,* results from the fact that a transistor in saturation has a saturation charge of excess minority carriers stored in the base. The transistor cannot respond until the saturation excess charge has been removed.

MULTIVIBRATORS

Multi means many; vibrator means oscillator. A circuit which can oscillate at a number of frequencies is called a multivibrator. Basically there are three types of multivibrators:

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the

states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators:

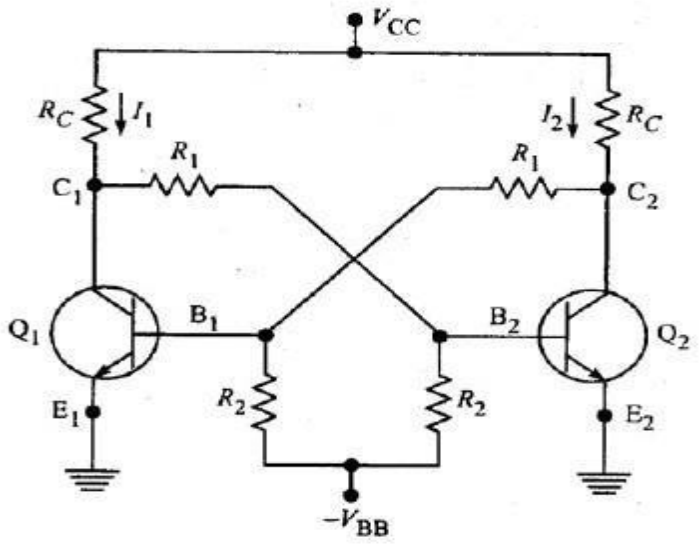
1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

A FIXED-BIAS BISTABLE MULTIVIBRATOR

The Figure below shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier.



In one of the stable states, transistor Q[is ON (i.e. in saturation) and Q2 is OFF (i.e. in cut-off), and in the other stable state Qj is OFF and Q2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents /[and 72 and suppose there is a minute fluctuation in the current *1*\~—let us say it increases by a small amount—then the voltage at the collector of Qi decreases. This will result in a decrease in voltage at the base of Q2. So Q2 conducts less and /2 decreases and hence the potential at the collector of Q2 increases. This results in an increase in the base potential of *Qi.* So, Qi conducts still more and /[is further increased and the potential at the collector of Qt is further reduced, and so on. So, the current *I*\ keeps on increasing and the current /2 keeps on decreasing till Q(goes into saturation and Q2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one. *A stable state of a binary is one in which the voltages and currents satisfy the Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.*

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is ir cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably Sometimes the drift may

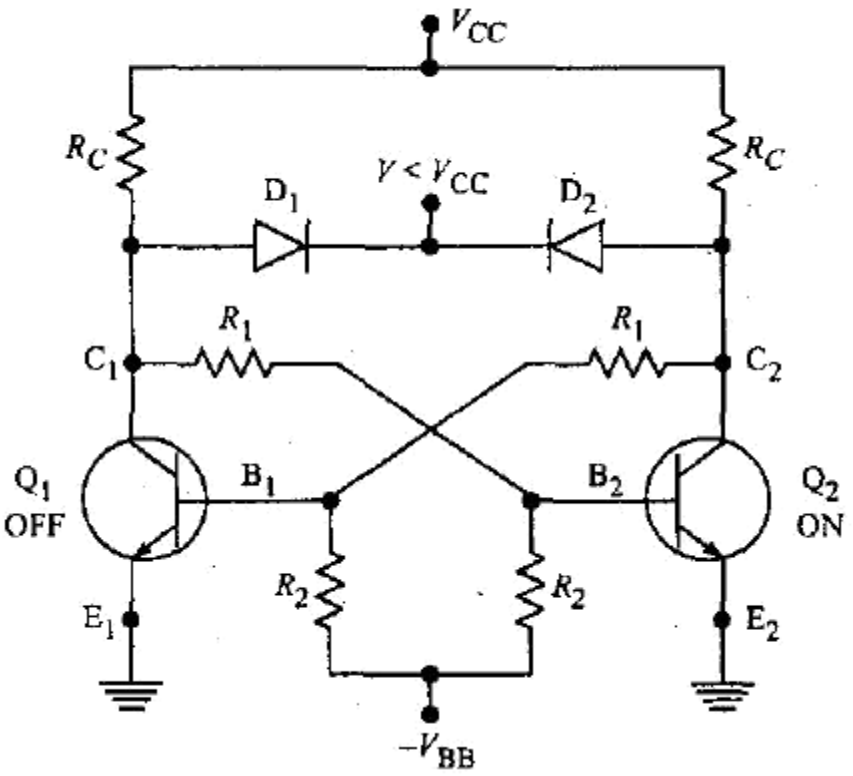
be so much that the device operating in the active region may gc into cut-off, and with both the devices in cut-off the circuit will be useless.

Selection of components in the fixed-bias bistable multivibrator

In the fixed-bias binary shown in Figure 4.1., nearly the full supply voltage Vcc will appear across the transistor that is OFF. Since this supply voltage *Vcc* is to be reasonably smaller than the collector breakdown voltage SVce. *Vcc* restricted to a maximum of a few tens of volts. Under saturation conditions the collector current *Ic* is maximum. Hence *RC* must be chosen so that this value of C (= VCC/^G) does not exceed the maximum permissible limit. The values of *R1, R2* and VBB must be selected such that in one stat>le state the base current is large enough to drive the transistor into saturation whereas in the second stable state the emitter junction must be below cut-off. The signal at a collector called the output swing Vw is the change in collector voltage resulting from a transistor going from one state to the other, i.e. Vw = VCi - IC2- If the loading caused by *RI* can be neglected, then the collector voltage of the OFF transistor is *Vcc.* Since the collector saturation voltage is few tenths of a volt, then the swing Vw = *Vcc,* independently of *RQ*- The component values, the supply voltages and the values of /CBO, *h^,* VBE(sat), and VCE(sat) are sufficient for the analysis of transistor binary circuits.

Loading

The bistable multivibrator may be used to drive other circuits and hence at one or both the collectors there are shunting loads, which are not shown in Figure 4.1. These loads reduce the magnitude of the collector voltage VC1 of the OFF transistor. This will result in reduction of the output voltage swing. A reduced VC[will decrease VB2 and it is possible that Q2 may not be driven into saturation- Hence the flip-flop circuit components must be chosen such that under the heaviest load, which the binary drives, one- transistor remains in saturation while the other is in cut-off. Since the resistor *RI* also loads the OFF transistor, to reduce loading, the value of *R]* should be as large as possible compared to the value of *Rc.* But to ensure a loop gain in excess of unity during the transition between the states, *R^* should be selected such that For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing V\v = V, arid a constant base saturation current *IB2* can be obtained by clamping the collectors to an auxiliary voltage V < Vcc through the diodes *DI* and D2 as indicated in Figure 4.2. As Qi cuts OFF, its collector voltage rises and when it reaches *V,* the "collector catching diode" D| conducts and clamps the output to *V.*



Standard specifications

In the cut-off region, i.e. for the OFF state

V_{BE} (cut-off) : $\leq$ 0 V for silicon transistor
$\leq$ – 0.1 V for germanium transistor

In the saturation region, i.e. for the ON state

V_{BE} (sat) : 0.7 V for silicon transistor
0.3 V for germanium transistor
V_{CE} (sat) : 0.3 V for silicon transistor
0.1 V for germanium transistor

The above values hold good for n-p-n transistors. For p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation

To test whether a transistor is really in saturation or not evaluate the collector current i_C and the base current i_B independently.

If $i_B > i_B$ (min), where i_B (min) = i_C/h_{FE} (min) the transistor is really in saturation.
If $i_B \leq i_B$ (min), the transistor is not in saturation.

Test for cut-off

To test whether a transistor is really cut-off or not, find its base-to-emitter voltage. If V_{BE} is negative for an n-p-n transistor or positive for a p-n-p transistor, the transistor is really cut-off.

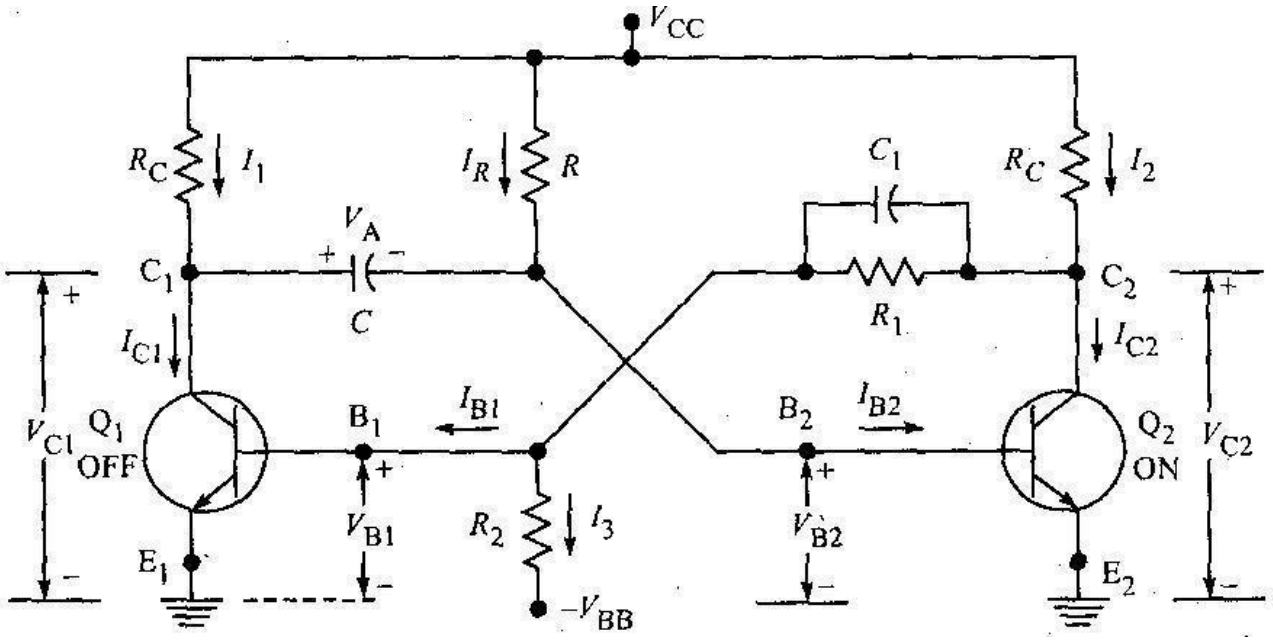
MONOSTABLE MULTIVIBRATOR

Monostable Multivibrators have only **one** stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Monostable multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state, which is determined by the time constant of the timing capacitor, CT and the resistor, RT until it resets or returns itself back to its original (stable) state. It will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, **Monostable Multivibrators** have only **ONE** stable state and go through a full cycle in response to a single triggering input pulse.

THE COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-to-base coupled (simply called collectorcoupled) monostable multivibrator using n-p-n transistors. The collector of Q2 is coupled to the base of Qi by a resistor *R}* (dc coupling) and the collector of Qt is coupled to the base of Q2 by a capacitor *C* (ac coupling). Ci is the commutating capacitor introduced to increase the speed of operation. The base of Qi is connected to -VBB through a resistor *R2,* to ensure that Q! is cut off under quiescent conditions. The base of Q2 is connected to VCc through *R* to ensure that Q2 is ON under quiescent conditions. In fact, *R* may be returned to even a small positive voltage but connecting it to *Vcc* is advantageous. The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q2ON (i.e. in saturation) and Q! OFF (i.e. in cut-off)- The multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q2 or at the collector of Q|. Since the triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed. When a negative signal is applied at the base of Q2 at $t \sim 0$, due to regenerative action Q2 goes to OFF state and Qi goes to ON state. When Q, is ON, a current /i flows through its *Rc* and hence its collector voltage drops suddenly by *I\RC* This drop will be instantaneously



transmitted through the coupling capacitor C to the base of Q2. So at t = 0+ , the base voltage of Q2 is

$$V_{BE}(\text{sat}) - I_1 R_C$$

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time *T)* because when Qt conducts, the coupling capacitor *C* charges from Vcc through the conducting transistor Qi and hence the potential at the base of Q2 rises exponentially with a time constant

$(R + R_o)C \approx RC,$ where *R0* is the conducting transistor output impedance including the resistance *Rc.* When it passes the cut-in voltage Vy of Q2 (at a time *t = T),* a regenerative action takes place turning Q| OFF and eventually returning the multivibrator to its initial stable state. The transition from the stable state to the quasi-stable state takes place at *t* = 0, and the reverse transition from the quasi-stable state to the stable state takes place at *t = T.* The time *T* for which the circuit is in its quasi-stable state is also referred to as the delay time, and also as the gate width, pulse width, or pulse duration. The delay time may be varied by varying the time constant *t(= RC).*

Expression for the gate width T of a monostable multivibrator neglecting the reverse saturation current /CBO

The below Figure (a) shows the waveform at the base of transistor Q2 of the monostable multivibrator

For *t* < 0, Q2 is ON and so vB2 = VBE(sat). At *t* = 0, a negative signal applied brings Q2 to OFF state and Q[into saturation. A current I flows through *Rc* of Qt and hence vci drops abruptly by I c volts and so vB2 also drops by *I\RC* instantaneously. So at *t* - 0, vB2 = VBE(sat) - *I}RC.* For *t* > 0, the capacitor charges with a time constant *RC,* and hence the base voltage of Q2 rises exponentially towards VCc with the same time constant. At *t* = *T,* when this base voltage rises to the cut-in voltage level Vy of the transistor, Q2 goes to ON state, and Qj to OFF state and the pulse ends. In the interval 0 < *t* < 7", the base voltage of Q2, i.e. vB2 is given by

$$v_{B2} = V_{CC} - (V_{CC} - \{V_{BE}(\text{sat}) - I_1 R_C\})e^{-t/\tau}$$

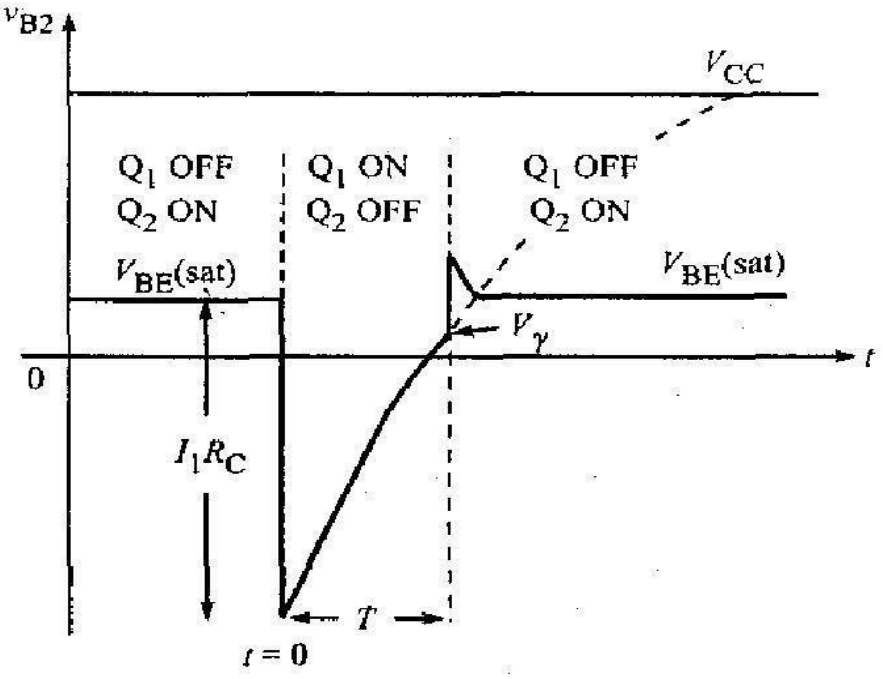


Fig a) Voltage variation at the base of Q2 during the quasi-stable state

But $I_1 R_C = V_{CC} - V_{CE}(\text{sat})$ (because at $t = 0^-$, $v_{C1} = V_{CC}$ and at $t = 0^+$, $v_{C1} = V_{CE}(\text{sat})$)

$$\therefore \quad v_{B2} = V_{CC} - [V_{CC} - \{V_{BE}(\text{sat}) - (V_{CC} - V_{CE}(\text{sat}))\}]e^{-t/\tau}$$

$$= V_{CC} - [2V_{CC} - \{V_{BE}(\text{sat}) + V_{CE}(\text{sat})\}]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V_{CC} - [2V_{CC} - \{V_{CE}(\text{sat}) + V_{BE}(\text{sat})\}]e^{-T/\tau}$$

i.e. $$e^{T/\tau} = \frac{2V_{CC} - [V_{CE}(\text{sat}) + V_{BE}(\text{sat})]}{V_{CC} - V_\gamma}$$

$$\therefore \quad \frac{T}{\tau} = \frac{\ln\left[2\left(V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right)\right]}{V_{CC} - V_\gamma}$$

i.e. $$T = \tau \ln 2 + \tau \ln \frac{V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}}{V_{CC} - V_\gamma}$$

Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction

$$V_\gamma = \frac{V_{CE}(sat) + V_{BE}(sat)}{2}$$

voltages for either Ge or Si transistors, i.e.

Neglecting the second term in the expression for *T*

$$T = \tau \ln 2$$

$$T = (R + R_a)C \ln 2 = 0.693(R + R_a)C$$

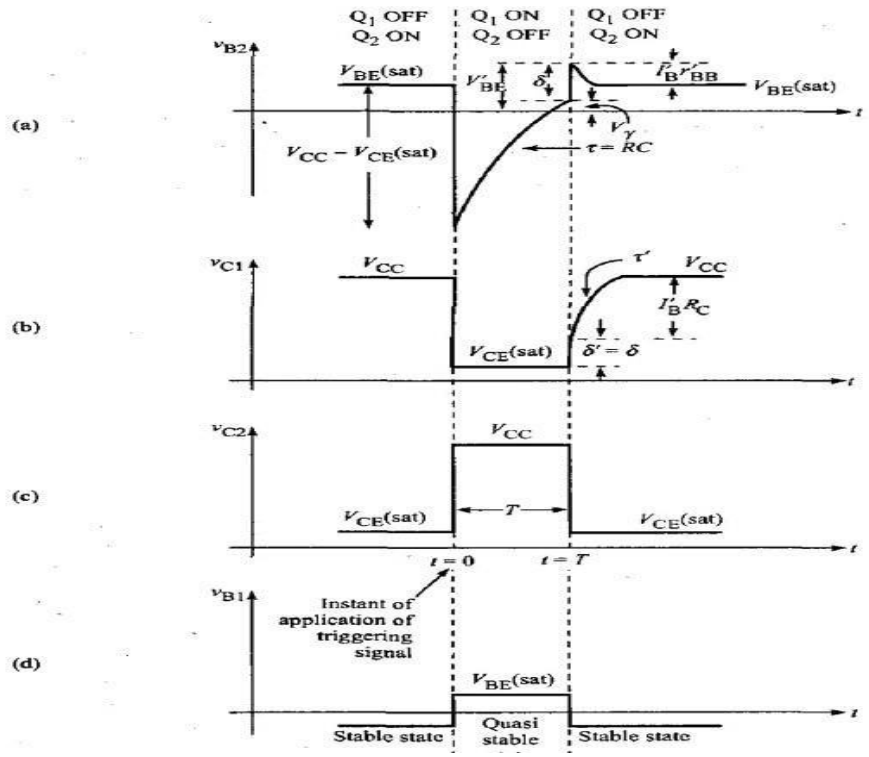
but for a transistor in saturation *Ra « R.*

Gate width, *T* = 0.693RC

The larger the *Vcc* is, compared to the saturation junction voltages, the more accura the result is. The gate width can be made very stable (almost independent of transistor characteristic supply voltages, and resistance values) if Q1 is driven into saturation during the quasi-stab state.

Waveforms of the collector-coupled monostable multivibrator

The waveforms at the collectors and bases of both the transistors Q1 and Q2 are shown below



(a) at the base of Q2, (b) at the collector of Q1, (c) at the collector of Q2, and (d) at the base of Q1

ASTABLE MULTIVIBRATOR

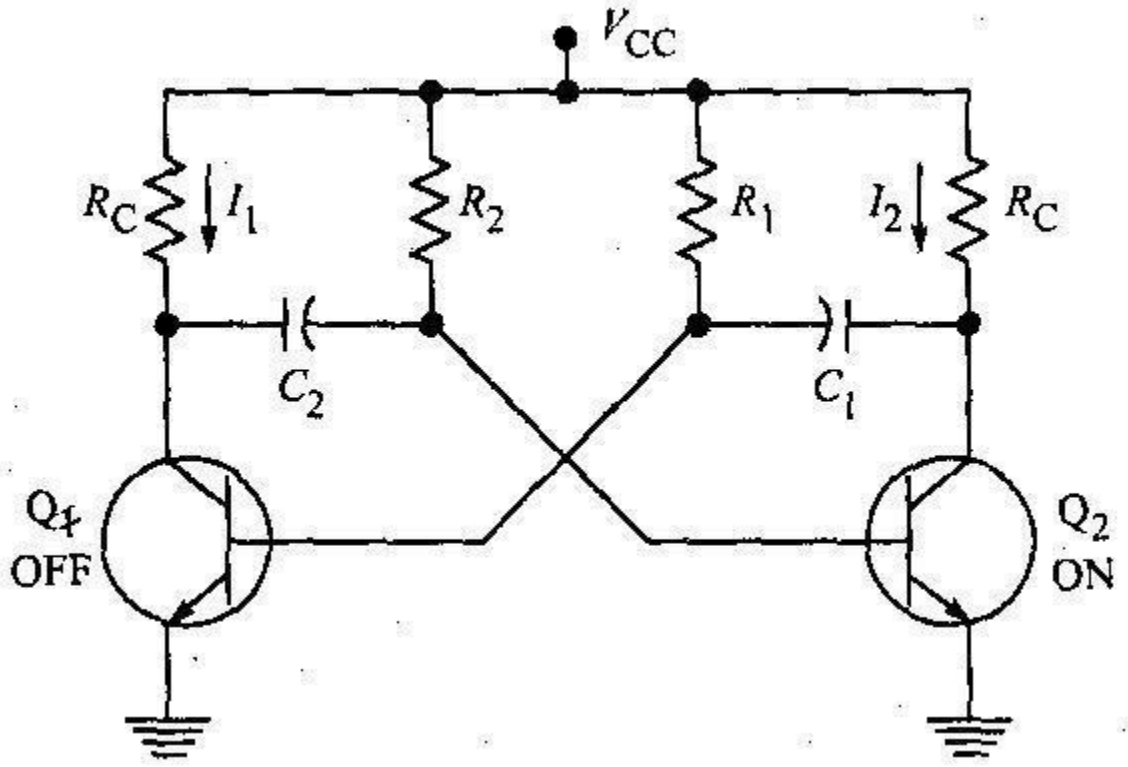
As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are two types of astable multivibrators:

1. Collector-coupled astable multivibrator
2. Emitter-coupled astable multivibrator

THE COLLECTOR-COUPLED ASTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-coupled astable multivibrator using n-p-n transistors. The collectors of both the transistors Qj and Q2 are connected to the bases



of the other transistors through the coupling capacitors Cs and C2. Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. No triggering signal is required for this multivibrator. The component values are selected such that, the moment it is connected to the supply, due to supply transients one

transistor will go into saturation and the other into cut-off, and also due to capacitive couplings it keeps on-oscillating between its two quasi stable states.

The waveforms at the bases and collectors for the astable multivibrator, are shown in below Figure. Let us say at $t = 0$, Q2 goes to ON state and Q] to OFF state. So, for $t < 0$, Q2 was OFF and Q1 was ON

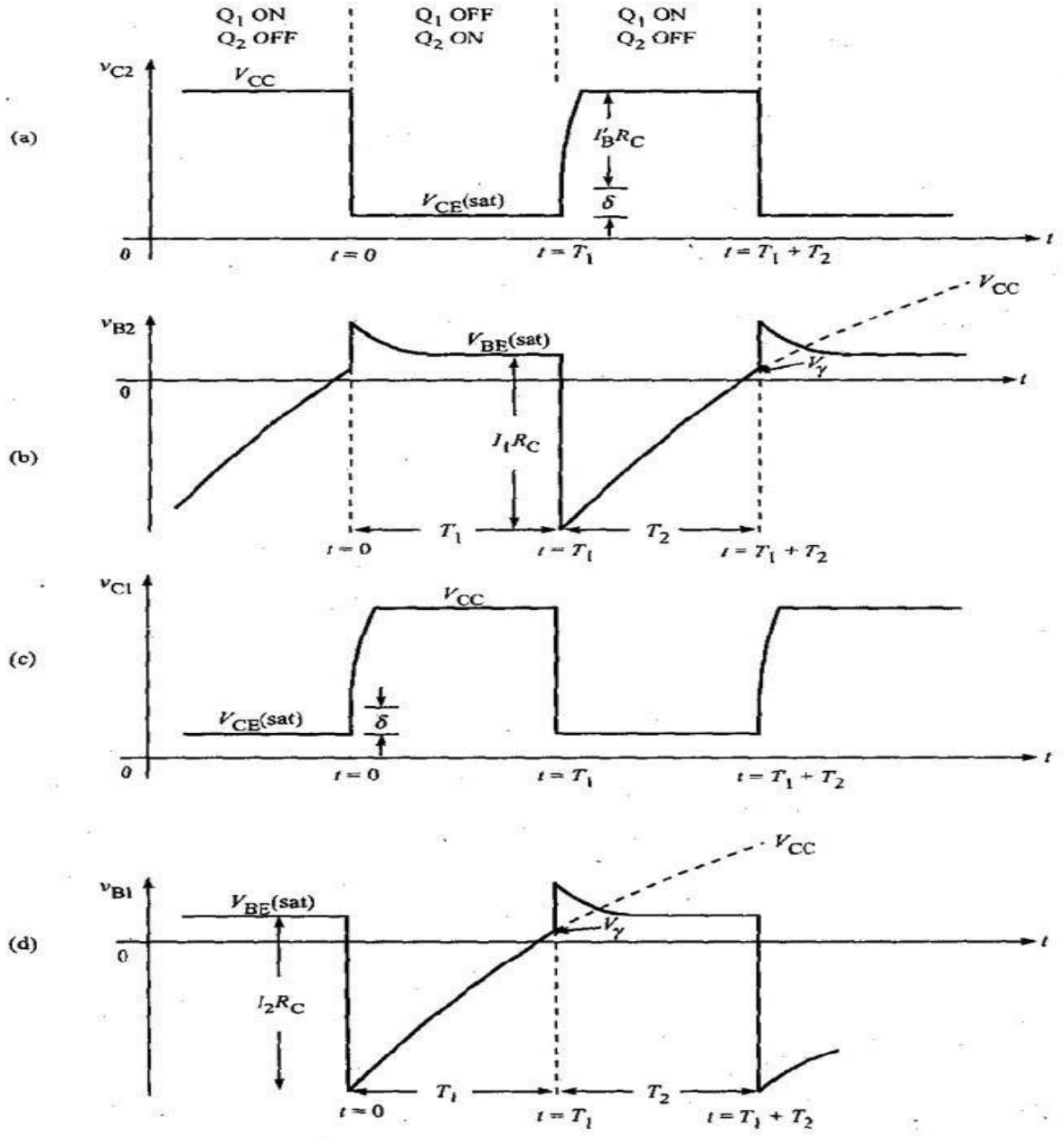


Fig: waveforms at the bases and collectors of a collector-coupled astable multivibrator

Hence for $t < 0$, vB2 is negative, vC2 = *Vcc,* VB! = VBE(sat) and vcj = VCE(sat). The capacitor C2 charges from Vcc through *R2* and vB2 rises exponentially towards V cc. At $t = 0$, vB2 reaches the cut-in voltage *Vy* and Q2 conducts. As Q2 conducts, its collector voltage Vc2 drops by /2/?c - ^cc ~ VcE(sa O- This drop in vc2 is transmitted to the base of Qj through the coupling capacitor C2

and hence vB1 also falls by /2/?c- Qi goes to OFF state. So, VB] = VBE(sat) - /2tfc, and its collector voltage vcl rises towards VCc- This rise in vc] is coupled through the coupling capacitor C2 to the base of Q2, causing an overshoot *§* in vB2 and the abrupt rise by the same amount *8* in VCL as shown in Figure 4.51(c). Now since Q2 is ON, *C*\ charges from *Vcc* through *Rlt* and hence VB] rises exponentially. At *t* = 7"], when VB! rises to *VY,* Qi conducts and due to regenerative action Qi goes into saturation and Q2 to cut-off. Now, for *t > T*\, the coupling capacitor C2 charges from Vcc through *R2* and at / = 7", + 7"2, when vB2 rises to the cut-in voltage Vr, Q2 conducts and due to regenerative feedback Q2 goes to ON state and Q| to OFF state. The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator. It is a free running oscillator.

Expression for the frequency of oscillation of an astable multivibrator

Consider the waveform at the base of Q_1 shown in Figure 4.54(d). At $t = 0$,

$$v_{B1} = V_{BE}(\text{sat}) - I_2R_C$$

But $$I_2R_C = V_{CC} - V_{CE}(\text{sat})$$

$\therefore$ $$\text{At } t = 0,\ v_{B1} = V_{BE}(\text{sat}) - V_{CC} + V_{CE}(\text{sat})$$

For $0 < t < T_1$, v_{B1} rises exponentially towards V_{CC} given by the equation,

$$v_o = v_f - (v_f - v_i)e^{-t/\tau}$$

$\therefore$ $$v_{B1} = V_{CC} - [V_{CC} - (V_{BE}(\text{sat}) - V_{CC} + V_{CE}(\text{sat}))]e^{-t/\tau_1}, \text{ where } \tau_1 = R_1C_1$$

At $t = T_1$, when v_{B1} rises to V_γ, Q_1 conducts

$\therefore$ $$V_\gamma = V_{CC} - [2V_{CC} - (V_{BE}(\text{sat}) + V_{CE}(\text{sat}))]e^{-T_1/R_1C_1}$$

or $$e^{T_1/R_1C_1} = \frac{2\left[V_{CC} - \dfrac{V_{BE}(\text{sat}) + V_{CE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln \frac{2\left[V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln 2 + R_1C_1 \ln \frac{\left[V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

At room temperature for a transistor,

$$V_\gamma \simeq \frac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}$$

$\therefore$ $$T_1 = R_1C_1 \ln 2 = 0.693R_1C_1$$

On similar lines considering the waveform of above Figure , we can show that the time *T2* for which Q2 is OFF and Q1 is ON is given by The period of the waveform, The frequency of oscillation, If *R{ = R2 = R,* and Cs = C2 = C, then TI = *T2* = T.

$$T = 2 \times 0.693RC = 1.386RC \qquad \text{and} \qquad f = \frac{1}{1.386RC}$$

The frequency of oscillation may be varied over the range from cycles to mega cycles by varying *RC.* It is also possible to vary the frequency electrically by connecting *R1* and *R2* to an auxiliary voltage source *V* (the collector supply remains +VCC) and then varying this voltage *V.*

THE EMITTER-COUPLED ASTABLE MULTIVIBRATOR

An emitter-coupled astable multivibrator may be obtained by using three power supplies or a single power supply. The below Figure (a) shows the circuit diagram of a free-running emitter coupled multivibrator using n-p-n transistors. Figure 4.64 shows its waveforms. Three power supplies are indicated for the sake of simplifying the analysis. A more practical circuit using a single supply is indicated in below Figure (b). Let us assume that the circuit operates in such a manner that Q1 switches between cut-off and saturation and Q2 switches between cut-off and its active region.

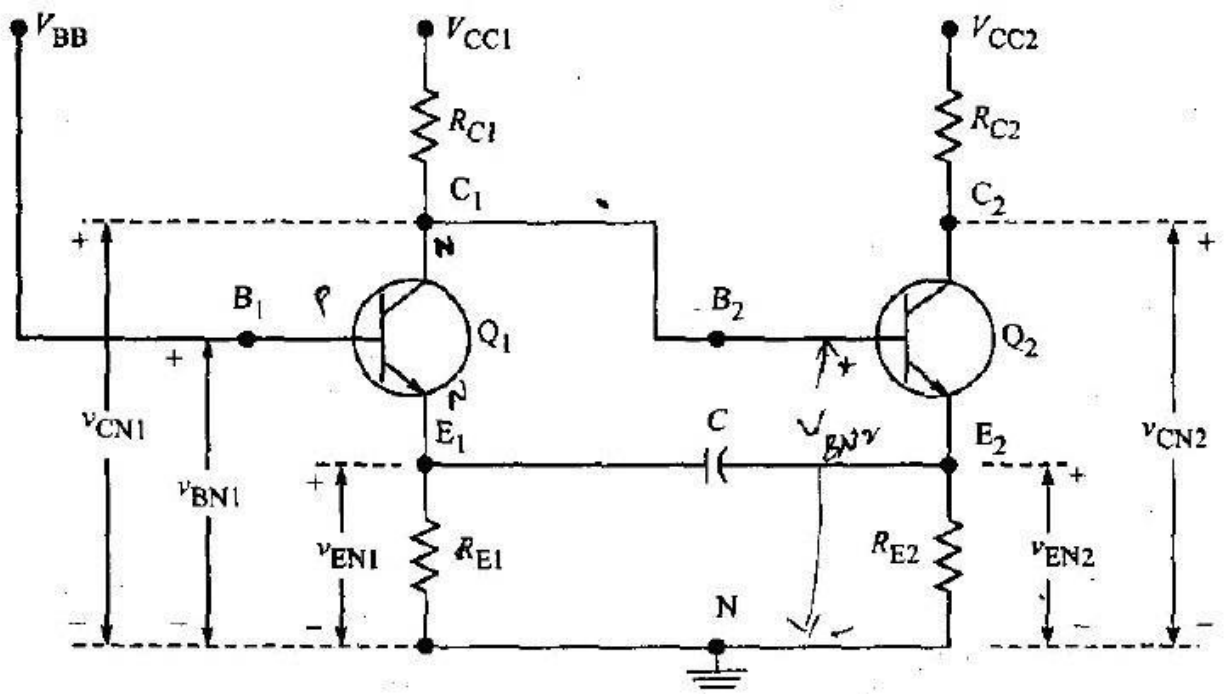


Fig a) Astable Emitter-Coupled Multivibrator

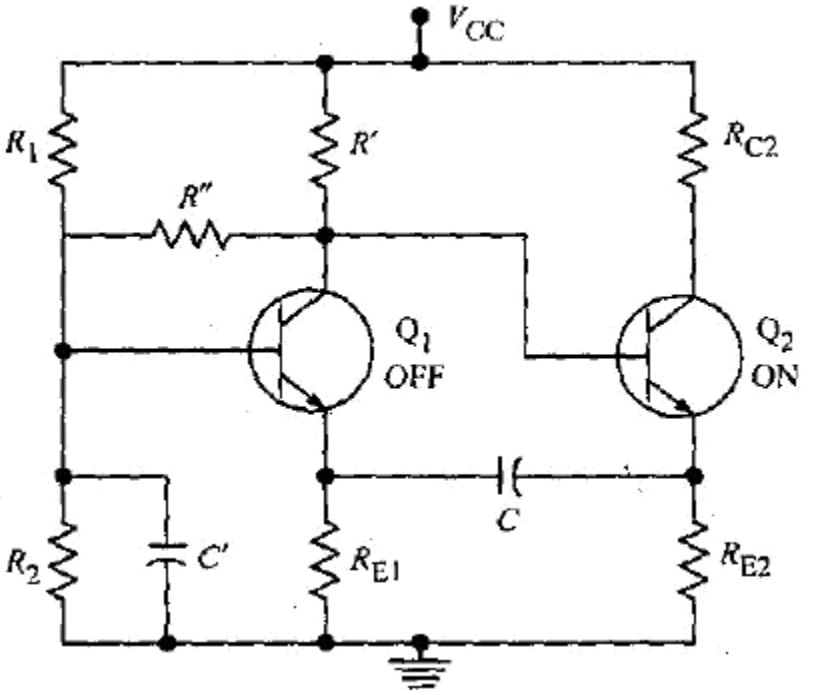


Fig b) Emitter Coupled multivibrator

The waveforms at the base and collector are as shown below:

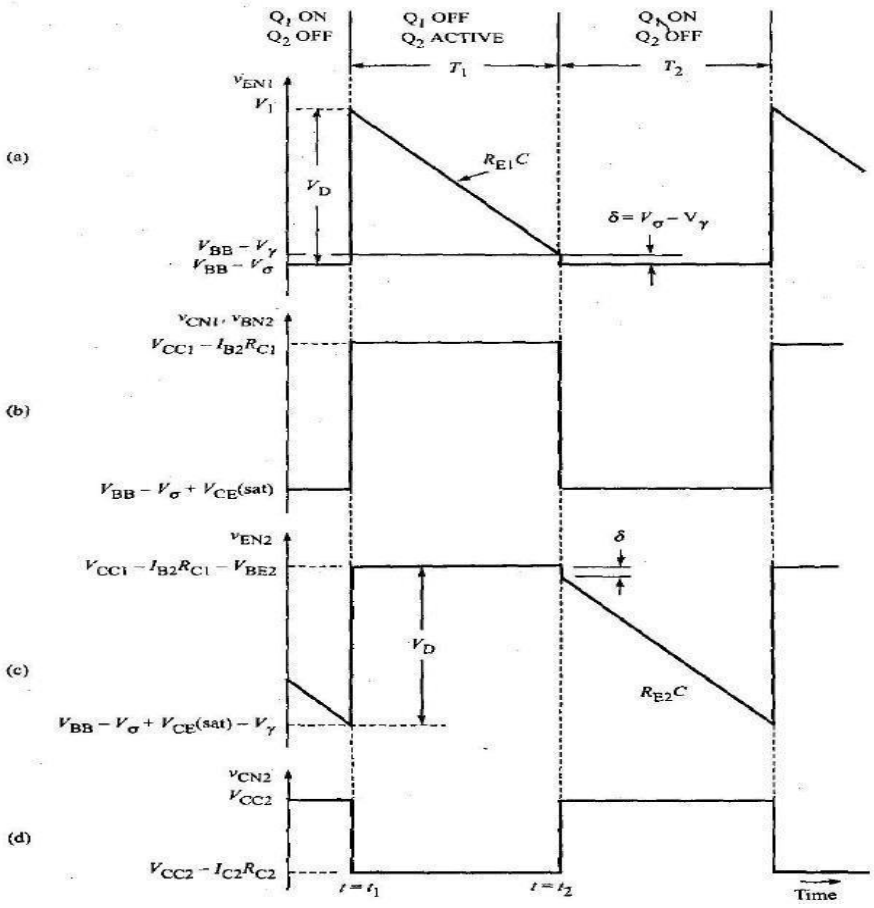


Fig waveforms of the emitter-coupled astable multivibrator

Advantages

1. It is inherently self-starting.
2. The collector of Q2 where the output is taken may be loaded heavily even capacitively.
3. The output is free of recovery transients.
4. Because it has an isolated input at the base of Q1, synchronization is convenient.
5. Frequency adjustment is convenient because only one capacitor is used.

Disadvantages

1. This circuit is more difficult to adjust for proper operating conditions.
2. This circuit cannot be operated with *T1* and T2 widely different.
3. This circuit uses more components than does the collector-coupled circuit.

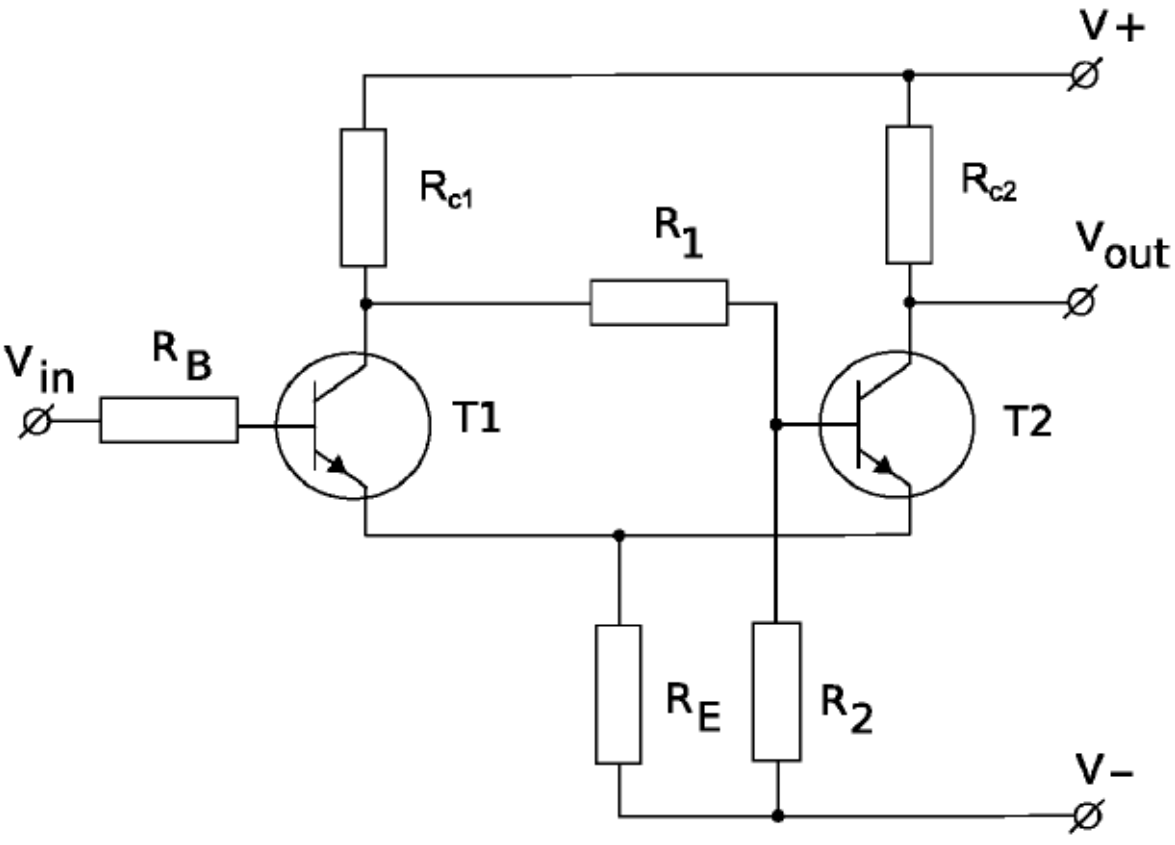
Schmitt trigger

In electronics, **Schmitt trigger** is a circuit with positive feedback and a loop gain >1. The circuit is named "trigger" because the output retains its value until the input changes sufficiently to trigger a change: in the non-inverting configuration, when the input is higher than a certain chosen threshold, the output is high; when the input is below a different (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. This dual threshold action is called *hysteresis* and implies that the Schmitt trigger possesses memory and can act as a bi-stable circuit (latch). There is a close relation between the two kinds of circuits: a Schmitt trigger can be converted into a latch and a latch can be converted into a Schmitt trigger. Schmitt trigger devices are typically used in open-loop controller configurations for noise immunity and closed loop negative feedback configurations to implement bi-stable regulators, triangle/square wave generators, etc.

The original Schmitt trigger is based on the dynamic threshold idea that is implemented by a voltage divider with a switchable upper leg (the collector resistors Rc1 and Rc2) and a steady lower leg (RE). T1 acts as a comparator with a differential input (T1 base-emitter junction) consisting of an inverting (T1 base) and a non-inverting (T1 emitter) inputs. The input voltage is applied to the inverting input; the output voltage of the voltage divider is applied to the non-inverting input thus determining its threshold. The comparator output drives the second common collector stage T2 (an *emitter follower*) through the voltage follower R1-R2. The emitter-coupled transistors T1 and T2 actually compose an electronic double throw switch that switches over the

upper legs of the voltage divider and changes the threshold in a different (to the input voltage) direction.

This configuration can be considered as a differential amplifier with series positive feedback between its non-inverting input (T2 base) and output (T1 collector) that forces the transition process. There is also a smaller negative feedback introduced by the emitter resistor RE. To make the positive feedback dominate over the negative one and to obtain a hysteresis, the proportion between the two collector resistors is chosen Rc1 > Rc2. Thus less current flows through and less voltage drop is across RE when T1 is switched on than in the case when T2 is switched on. As a result, the circuit has two different thresholds in regard to ground.



Schmitt trigger implemented by two emitter-coupled transistor stages

Operation:

Initial state. For NPN transistors as shown, imagine the input voltage is below the shared emitter voltage (high threshold for concreteness) so that T1 base-emitter junction is backward-biased and T1 does not conduct. T2 base voltage is determined by the mentioned divider so that T2 is conducting and the trigger output is in the low state. The two resistors Rc2 and RE form

another voltage divider that determines the high threshold. Neglecting VBE, the high threshold value is approximately

$$V_{HT} = \frac{R_E}{R_E + R_{c2}} V_+.$$

The output voltage is low but well above the ground. It is approximately equal to the high threshold and may not be low enough to be a logical zero for next digital circuits. This may require additional shifting circuit following the trigger circuit.

Crossing up the high threshold:

When the input voltage (T1 base voltage) rises slightly above the voltage across the emitter resistor RE (the high threshold), T1 begins conducting. Its collector voltage goes down and T2 begins going cut-off, because the voltage divider now provides lower T2 base voltage. The common emitter voltage follows this change and goes down thus making T1 conduct more. The current begins steering from the right leg of the circuit to the left one. Although T1 is more conducting, it passes less current through RE (since Rc1 > Rc2); the emitter voltage continues dropping and the effective T1 base-emitter voltage continuously increases. This avalanche-like process continues until T1 becomes completely turned on (saturated) and T2 turned off. The trigger is transitioned to the high state and the output (T2 collector) voltage is close to V+. Now, the two resistors Rc1 and RE form a voltage divider that determines the low threshold. Its value is approximately

$$V_{LT} = \frac{R_E}{R_E + R_{c1}} V_+.$$

Crossing down the low threshold:

With the trigger now in the high state, if the input voltage lowers enough (below the low threshold), T1 begins cutting-off. Its collector current reduces; as a result, the shared emitter voltage lowers slightly and T1 collector voltage rises significantly. R1-R2 voltage divider conveys this change to T2 base voltage and it begins conducting. The voltage across RE rises, further reducing the T1 base-emitter potential in the same avalanche-like manner, and T1 ceases to conduct. T2 becomes completely turned-on (saturated) and the output voltage becomes low again.

UNIT –IV
TIME BASE GENARATORS

TIME BASE GENERATORS

A time-base generator is an electronic circuit which generates an output voltage or current waveform, a portion of which varies linearly with time. Ideally the output waveform should be a ramp. Time-base generators may be voltage time-base generators or current time-base generators. A voltage time-base generator is one that provides an output voltage waveform, a portion of which exhibits a linear variation with respect to time. A current time-base generator is one that provides an output current waveform, a portion of which exhibits a linear variation with respect to time. There are many important applications of time-base generators, such as in CROs, television and radar displays, in precise time measurements, and in time modulation. The most important application of a time-base generator is in CROs. To display the variation with respect to time of an arbitrary waveform on the screen of an oscilloscope it is required to apply to one set of deflecting plates a voltage which varies linearly with time. Since this waveform is used to sweep the electron beam horizontally across the screen it is called the *sweep voltage* and the time-base generators are called the *sweep* circuits.

GENERAL FEATURES OF A TIME-BASE SIGNAL

Figure (a) shows the typical waveform of a time-base voltage. As seen the voltage starting from some initial value increases linearly with time to a maximum value after which it returns again to its initial value. The time during which the output increases is called the *sweep time* and the time taken by the signal to return to its initial value is called the *restoration time,* the *return time,* or *the flyback time.* In most cases the shape of the waveform during restoration time and the restoration time itself are not of much consequence. However, in some cases a restoration time which is very small compared with the sweep time is required. If the restoration time is almost zero and the next linear voltage is initiated the moment the present one is terminated then a saw-tooth waveform shown in (b) is generated. The waveforms of the type shown in Figures (a) and (b) are generally called sweep waveforms even when they are used in applications not involving the deflection of an electron beam. In fact, precisely linear sweep signals are difficult to generate by time-base generators and moreover nominally linear sweep signals may be distorted when transmitted through a coupling

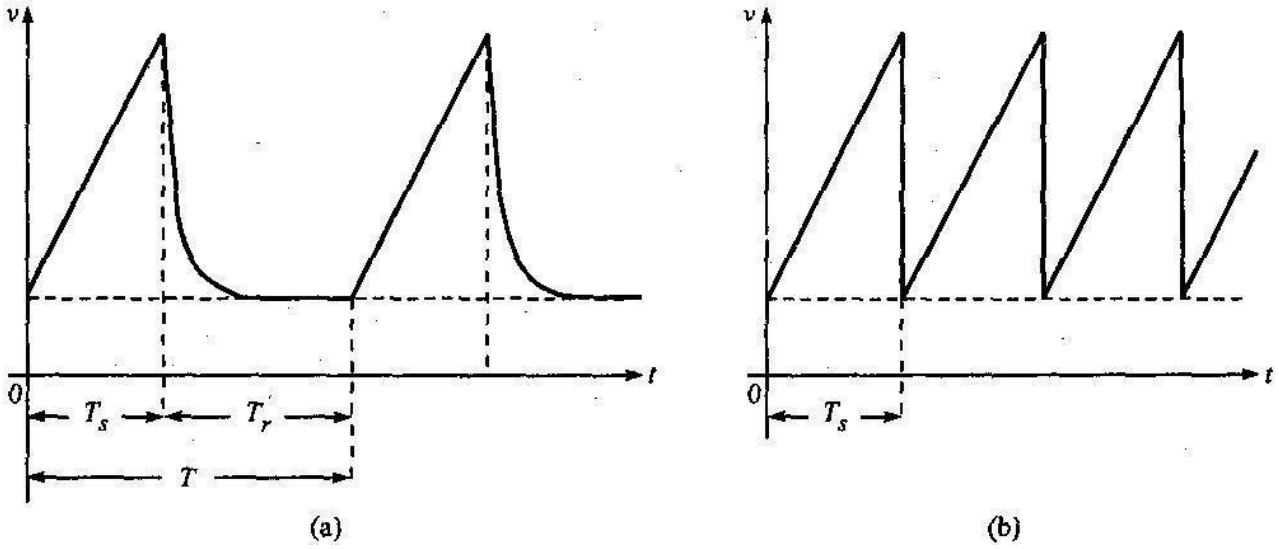


Fig 5.1 (a) General sweep voltage and (b) saw-tooth voltage waveforms.

The deviation from linearity is expressed in three most important ways:
1 . The slope or sweep speed error, *es*
2. The displacement error, *ed*
3. The transmission error, *et*

The slope or sweep-speed error, *es*

An important requirement of a sweep is that it must increase linearly with time, i.e. the rate of change of sweep voltage with time be constant. This deviation from linearity is defined as

$$\text{Slope or sweep-speed error, } e_s = \frac{\text{difference in slope at beginning and end of sweep}}{\text{initial value of slope}}$$

$$= \frac{\left.\frac{dv_0}{dt}\right|_{t=0} - \left.\frac{dv_0}{dt}\right|_{t=T_s}}{\left.\frac{dv_0}{dt}\right|_{t=0}}$$

The displacement error, *ed*

Another important criterion of linearity is the maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep. The displacement error *ed* is defined as

$$e_d = \frac{\text{maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep}}{\text{amplitude of the sweep at the end of the sweep time}}$$

$$= \frac{(v_s - v_s')_{\max}}{V_s}$$

As shown in Figure (a), *vs* is the actual sweep and *v's* is the linear sweep.

The transmission error, *et*

When a ramp signal is transmitted through a high-pass circuit, the output falls away from the input as shown in Figure (b). This deviation is expressed as transmission error *et,* defined as the difference between the input and the output divided by the input at the end of the sweep

$$e_t = \frac{V_s' - V_s}{V_s'}$$

where as shown in Figure (b), *V's* is the input and *Vs* is the output at the end of the sweep, i.e. at *t* = TS

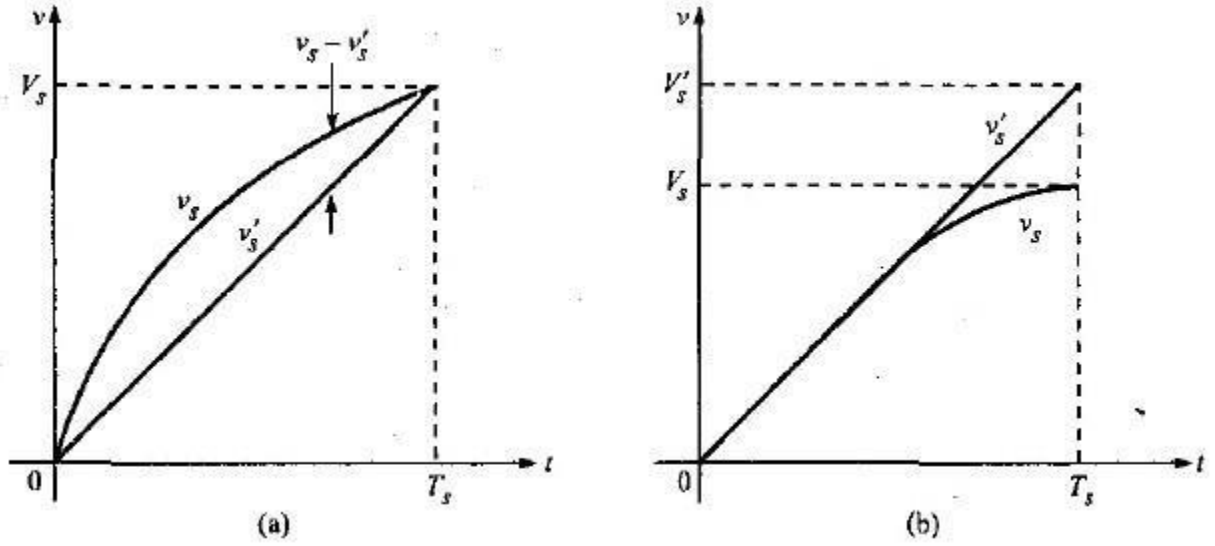


Fig.5.2 (a) Sweep for displacement error and (b) sweep for transmission error

If the deviation from linearity is small so that the sweep voltage may be approximated by the sum of linear and quadratic terms in *t,* then the above three errors are related as :

$$e_d = \frac{e_s}{8} = \frac{e_t}{4}$$

$$e_s = 2e_t = 8e_d$$

which implies that the sweep speed error is the more dominant one and the displacement error is the least severe one.

METHODS OF GENERATING A TIME-BASE WAVEFORM

In time-base circuits, sweep linearity is achieved by one of the following methods.

1. ***Exponential charging.*** In this method a capacitor is charged from a supply voltage through a resistor to a voltage which is small compared with the supply voltage.

2. ***Constant current charging***. In this method a capacitor is charged linearly from a constant current source. Since the charging current is constant the voltage across the capacitor increases linearly.

3. ***The Miller circuit***. In this method an operational integrator is used to convert an input step voltage into a ramp waveform.

4. ***The Phantastron circuit***. In this method a pulse input is converted into a ramp. This is a version of the Miller circuit.

5. ***The bootstrap circuit***. In this method a capacitor is charged linearly by a constant current which is obtained by maintaining a constant voltage across a fixed resistor in series with the capacitor.

6. ***Compensating networks***. In this method a compensating circuit is introduced to improve the linearity of the basic Miller and bootstrap time-base generators.

7. ***An inductor circuit***. In this method an *RLC* series circuit is used. Since an inductor does not allow the current passing through it to change instantaneously, the current through the capacitor more or less remains constant and hence a more linear sweep is obtained.

MILLER AND BOOTSTRAP TIME-BASE GENERATORS—BASIC PRINCIPLES

The linearity of the time-base waveforms may be improved by using circuits involving feedback. Figure 5.3 (a) shows the basic exponential sweep circuit in which S opens to form the sweep. A linear sweep cannot be obtained from this circuit because as the capacitor charges, the charging current decreases and hence the rate at which the capacitor charges, i.e. the slope of the output waveform decreases. A perfectly linear output can be obtained if the initial charging current / = *VIR* is maintained constant. This can be done by introducing an auxiliary variable generator v whose generated voltage v is always equal to and opposite to the voltage across the capacitor as shown in Figure 5.3 (b). Two methods of simulating the fictitious generator are discussed below

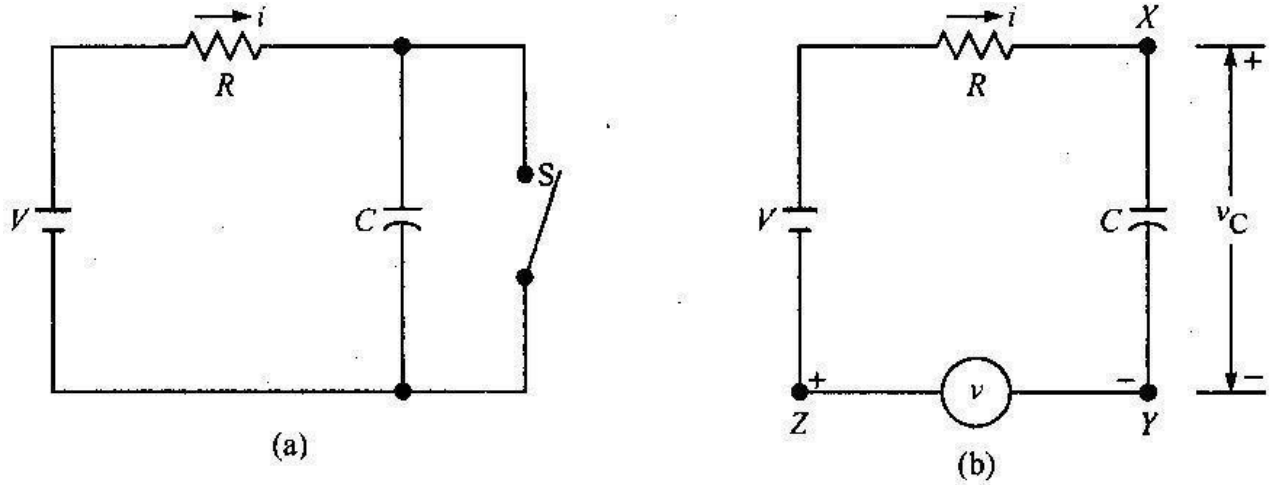


Fig. 5.3 (a) The current decreases exponentially with time and (b) the current remains constant

In the circuit of Figure 5.3 (b) suppose the point Z is grounded as in below Figure 5.4 (a). A linear sweep will appear between the point Y and ground and will increase in the negative direction. Let us now replace the fictitious (imaginary) generator by an amplifier with output terminals YZ and input terminals XZ as shown in below Figure 5.4 (b). Since we have assumed that the generated voltage is always equal and opposite to the voltage across the capacitor,

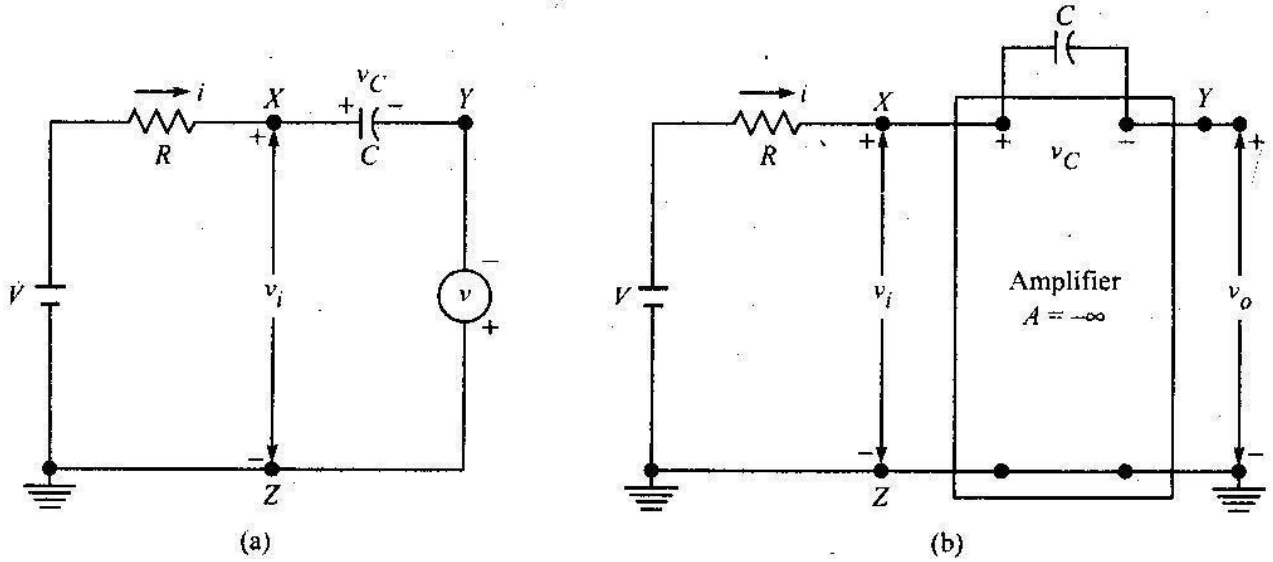


Fig. 5.4 (a) Figure 5.3(b) with Z grounded and (b) Miller integrator circuit.

the voltage between X and Z is equal to zero. Hence the point X acts as a virtual ground. Now for the amplifier, the input is zero volts and the output is a finite negative value. This can be achieved by using an operational integrator with a gain of infinity. This is normally referred to as the Miller integrator circuit or the Miller sweep. Suppose that the point Y in Figure 5.3(b) is grounded and the output is taken at Z. A linear sweep will appear between Z and ground and will increase in the positive direction. Let us now replace the fictitious generator by an amplifier with input terminals XY and output terminals ZY as shown in Figure 5.5. Since we have assumed that the generated voltage v at any instant is equal to the voltage across the capacitor vc, then *v0* must be equal to v,-, and the amplifier voltage gain must be equal to unity. The circuit of Figure 5.5 is referred to as the Bootstrap sweep circuit.

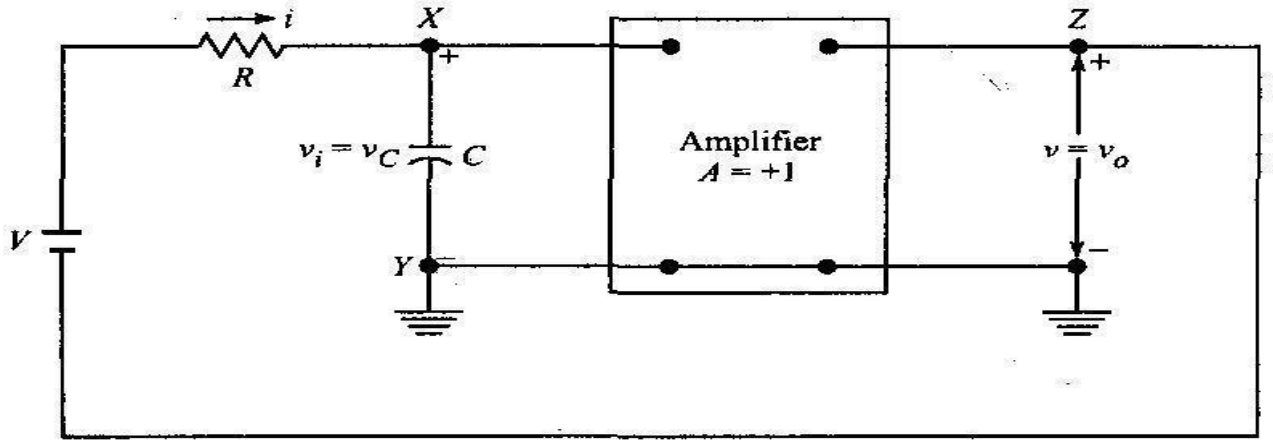


Fig. 5.5 Bootstrap sweep circuit.

The Miller sweep

The Miller integrating circuit of Figure 5.4 (b) is redrawn in Figure 5.6(a). A switch S at the closing of which the sweep starts is included. The basic amplifier has been replaced at the input side by its input resistance and on the output side by its Thevenin's equivalent. *R0* is the output resistance of the amplifier and *A* its open circuit voltage gain. Figure 5.6 (b) is obtained by replacing *V, R* and tf, on the input side by a voltage source *V* in series with a resistance *R'* where

$$V' = V\frac{R_i}{R_i + R} = \frac{V}{1 + \frac{R}{R_i}} \quad \text{and} \quad R' = R \| R_i = \frac{RR_i}{R + R_i}$$

Neglecting the output resistance in the circuit of Figure 5.6 {b), if the switch is closed at *t* = 0 and if the initial voltage across the capacitor is zero, then *v0* (f = 0+) = 0, because at / = 0~, V; ~ 0 and since the voltage across the capacitor cannot change instantaneously.

$$\text{At } t = 0^+, \qquad v_i - Av_i = 0 \qquad \text{or} \qquad v_i = Av_i = v_o = 0$$

This indicates that the sweep starts from zero.

At *t* = ∞, the capacitor acts as an open-circuit for dc. So no current flows and therefore

$$v_i = V' \qquad \text{and} \qquad v_o = AV'$$

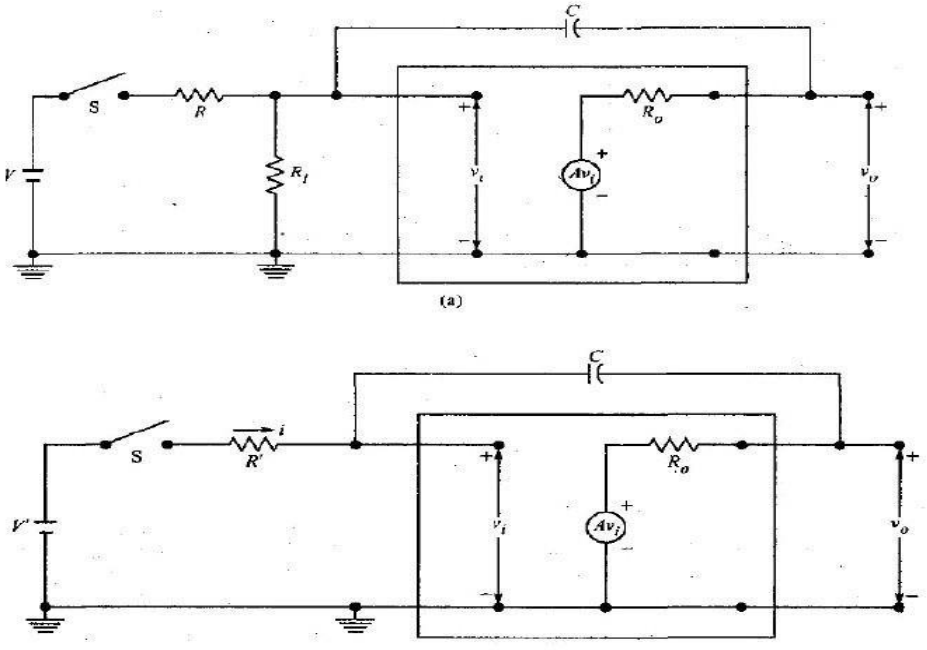


Fig. 5.6 (a) A Miller integrator with switch S, input resistance *Rf* and Thevenin's equivalent on the output side and (b) Figure 5.6(a) with input replaced by Thevenin's equivalent.

This indicates that the output is exponential and the sweep is negative-going since *A* is a negative number.

$$\text{Slope error, } e_s = \frac{V_s}{V}$$

where *Vs* is the sweep amplitude and *V* is the peak-to-peak value of the output

$$e_s(\text{miller}) = \frac{V_s}{|A|V'} = \frac{V_s}{|A|} \cdot \frac{R_i + R}{VR_i} = \frac{V_s}{V} \cdot \frac{1 + \dfrac{R}{R_i}}{|A|}$$

The deviation from linearity is $\dfrac{1 + \dfrac{R}{R_i}}{|A|}$ times that of an *RC* circuit charging directly from a source *V.* If *R0* is taken into account, the final value attained by *v0* remains as before, *AV* = - \A\V. The initial value however is slightly different.

To find *v0* at *t* = 0+ , writing the KVL around the mesh in Figure 5.13(b), assuming zero voltage across the capacitor, we have

$$V' - R'i - R_o i - Av_i = 0$$

$$v_i = V' - R'i$$

From the above equations, we find

$$v_i(t = 0^+) = \Delta v_i = v_o(t = 0^+) = \Delta v_o = \frac{\left(\dfrac{R_o}{R'}\right)V'}{1 - A + \dfrac{R_o}{R'}}$$

$$v_i(t = 0^+) \approx \frac{R_o V'}{R'|A|}$$

Therefore, if *R0* is taken into account, *v0(t* = 0+) is a small positive value and still it will be a negative going sweep with the same terminal value. Thus the negative-going ramp is preceded by a small positive jump. Usually this jump is/small compared to the excursion *AV',* Hence, improvement in linearity because of the increase in total excursion is negligible.

The bootstrap sweep

Figure 5.7 shows the bootstrap circuit of Figure 5.5. The switch S at the opening of which the sweep starts is in parallel with the capacitor *C.* Here, Ri,- is the input resistance, *A* is the open-circuit voltage gain, and *R0* is the output resistance of the amplifier.

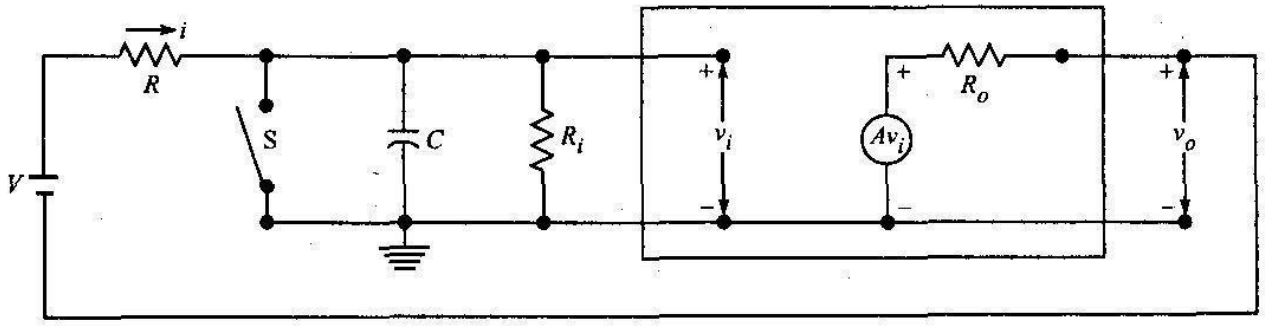


Fig. **5.7 Bootstrap** circuit of Figure 5.5 with switch S which opens at (= 0, input resistance *Rf,* and Thevenin's equivalent of the amplifier on the output side.

At *t* = 0~, the switch was closed and so *vt* - 0, Since the voltage across the capacitor cannot change instantaneously, at *t* = 0* also, v(- = 0 and hence Av, = 0, and the circuit shown in Figure 5.8 results.

$$t = 0^+, \qquad v_o = -V\frac{R_o}{R + R_o}$$

The output has the same value at *t* = 0 and hence there is no jump in the output voltage at *t* = 0.

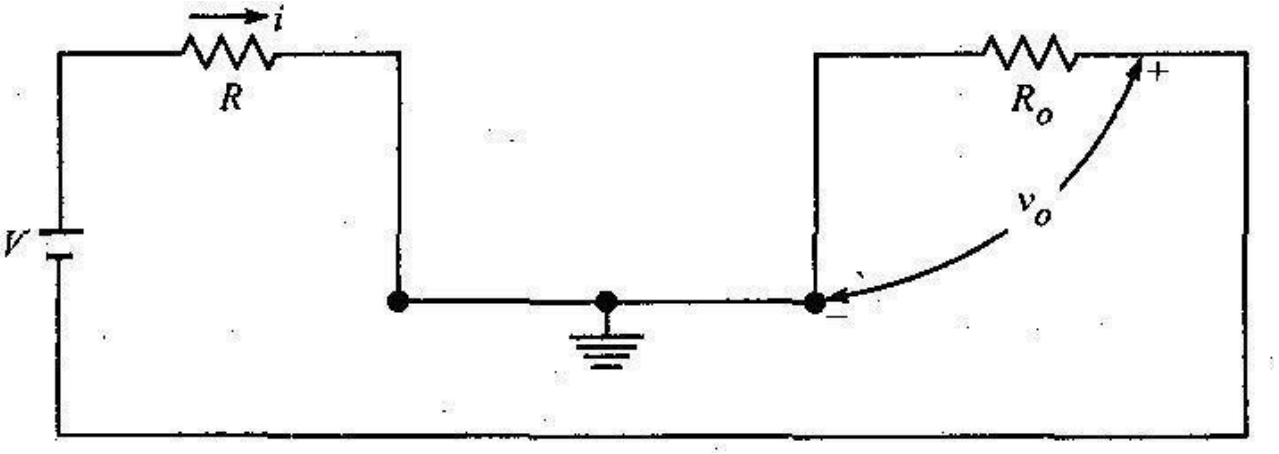


Fig.5.8 Equivalent circuit of Figure 5.7 aU = 0.

At *t* = ∞, the capacitor acts as an open-circuit and the equivalent circuit shown in Figure 5.9 results.

$$v_o(t = \infty) = AV_i - iR_o = AiR_i - iR_o = i(AR_i - R_o)$$

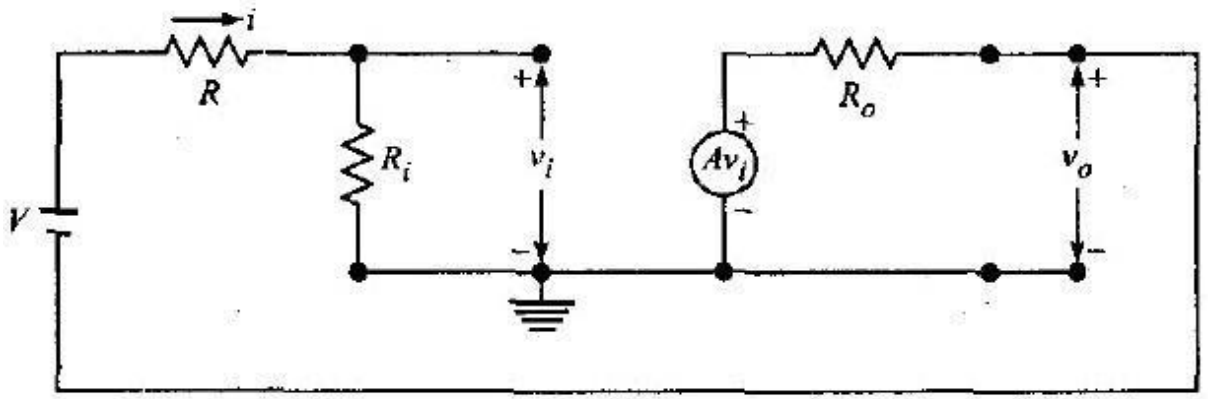


Fig 5.9 Equivalent circuit of Fig.5.7 at t= ∞

Writing KVL in the circuit of Figure 5.9,

$$V - iR - iR_i + AV_i - iR_o = 0$$

i.e.
$$i = \frac{V}{R + R_o + R_i(1 - A)}$$

$\therefore$
$$v_o(t = \infty) = \frac{V(AR_i - R_o)}{R + R_o + R_i(1 - A)}$$

Since *A* « 1, and if *R0* is neglected, we get

$$v_o(t = \infty) = \frac{V}{(1 - A) + \frac{R}{R_i}}$$

$$v_o(t = \infty) - v_o(t = 0) = \frac{V}{(1 - A) + \frac{R}{R_i}}$$

$$e_s(\text{bootstrap}) = \frac{\text{Sweep amplitude}}{\text{Total excursion of output}} = \frac{V_s}{V\left[(1 - A) + \frac{R}{R_i}\right]} = \frac{V_s}{V}\left(1 - A + \frac{R}{R_i}\right)$$

This shows that the slope error is [1 - *A* + *(R/Rj)]* times the slope error that would result if the capacitor is charged directly from *V* through a resistor.

Comparing the expressions for the slope error of Miller and bootstrap circuits, we can see that it is more important to keep *R/Rj* small in the bootstrap circuit than in the Miller circuit. Therefore, the Miller integrator has some advantage over the bootstrap circuit in that in the Miller circuit higher input impedance is less important.

THE TRANSISTOR MILLER TIME-BASE GENERATOR

Figure 5.10 shows the circuit diagram of a transistor Miller time-base generator. It consists of a three stage amplifier. To have better linearity, it is essential that a high input impedance amplifier be used for the Miller integrator circuit. Hence the first stage of the amplifier of Figure 5.10 is an emitter follower. The second stage is a common-emitter amplifier and it provides the necessary voltage amplification. The third stage (output stage) is also an emitter follower for two reasons. First, because of its low output impedance *R0* it can drive a load such as the horizontal amplifier. Second, because of its high input impedance it does not load the collector circuit of the second stage and hence the gain of the second stage can be very high. The capacitor C placed between the base of Qi and the emitter of Q3 is the timing capacitor. The sweep speed is changed from range to range by switching *R* and *C* and may be varied continuously by varying VBB.

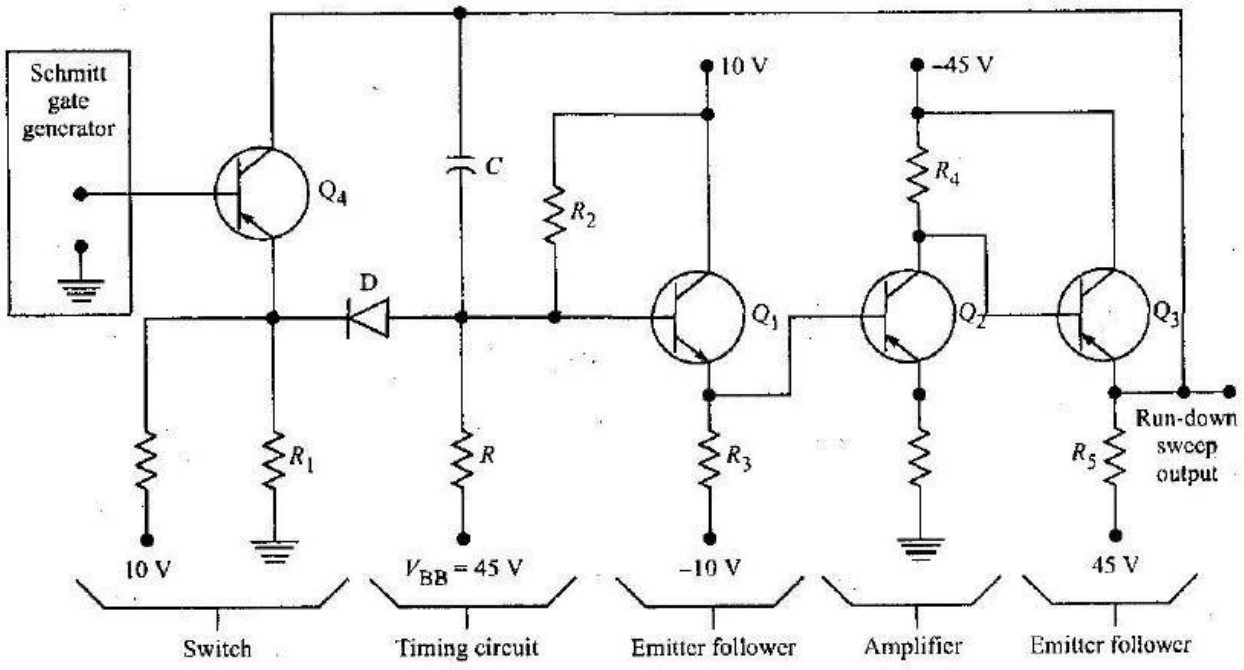


Fig.5.10 A Transistorized Miller Time-Base Generator

Under quiescent condition, the output of the Schmitt gate is at its lower level. So transistor Q4 is ON. The emitter current of Q4 flows through *RI* and hence the emitter is at a negative potential. Therefore the diode D conducts. The current through *R* flows through the diode D and the transistor Q4. The capacitor *C* is bypassed and hence is prevented fromcharging.

When a triggering signal is applied, the output of the Schmitt gate goes to its higher level. So the base voltage of Q4 rises and hence the transistor Q4 goes OFF. A current flows now from 10 V source through *RI.* The positive voltage at the emitter of Q4 now makes the diode D reverse biased. At this time the upper terminal of *C* is connected to the collector of Q4 which is in cut-off. The capacitor gets charged from VBB and hence a run down sweep output is obtained at the emitter of Q3. At the end of the sweep, the capacitor *C* discharges rapidly through D and Q4. Considering the effect of the capacitance *C\,* the slope or sweep speed error is given by

$$e_s = \frac{V_s}{V}\left(1 - A + \frac{R}{R_i} + \frac{C}{C_1}\right)$$

THE TRANSISTOR BOOTSTRAP TIME-BASE GENERATOR

Figure 5.11 shows a transistor bootstrap time-base generator. The input to transistor Q1 is the gating waveform from a monostable multivibrator (it could be a repetitive waveform like a square wave). Figure 5.12(a) shows the base voltage of Q1. Figure 5.12(b) shows the collector current waveform of Q1 and Figure 5.12(c) shows the output voltage waveform at the emitter of Q2

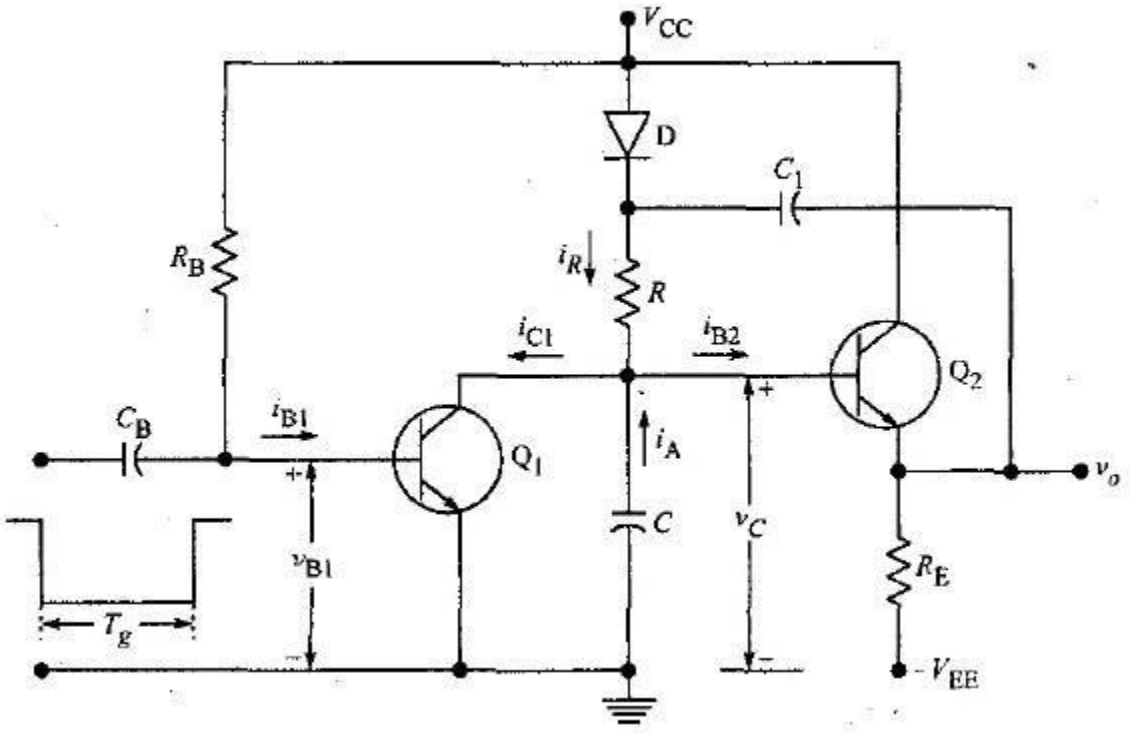


Fig.5.11 A Voltage Time Base Generator

Under quiescent conditions, i.e. before the application of the gating waveform at *t* - 0, Q| is in saturation because it gets enough base drive from *YCC* through ^B- So the voltage across the

capacitor which is also the voltage at the collector of Qj and the base of Q2 is VCE (sat). Since Q2 is conducting and acting as an emitter follower, the voltage at the emitter of Q2 which is also the output voltage is less than this base

voltage by VBE2, i.e. $v_o = V_{CE(sat)} - V_{BE2}$

is a small negative voltage (a few tenths of a volt negative). If we neglect this small voltage as well as the small drop across the diode D, then the voltage across *C*\ as well as across *R* is Vcc-Hence the current i> through *R* i§ *Vcc/R*- Since the quiescent output voltage at the emitter of Q2 is close to zero, the emitter current of Q2.

Hence the base current of Q2 is

iB2 = VEE /

hFE RE iR = iC1 + iB2

Since the base current of Q2, i.e. IB2 is very small compared with the collector current iC1 of Q1

$$i_{C1} \approx i_R \approx \frac{V_{CC}}{R}$$

For Q1 to be really in saturation under quiescent condition, its base current ((iB = *VCC/RB)* t be at least equal to 'IChFE> i.e. VCC//hFE^. so that

$$\frac{V_{CC}}{R_B} > \frac{V_{CC}}{h_{FE}R} \qquad \text{i.e.} \qquad R_B < h_{FE}R$$

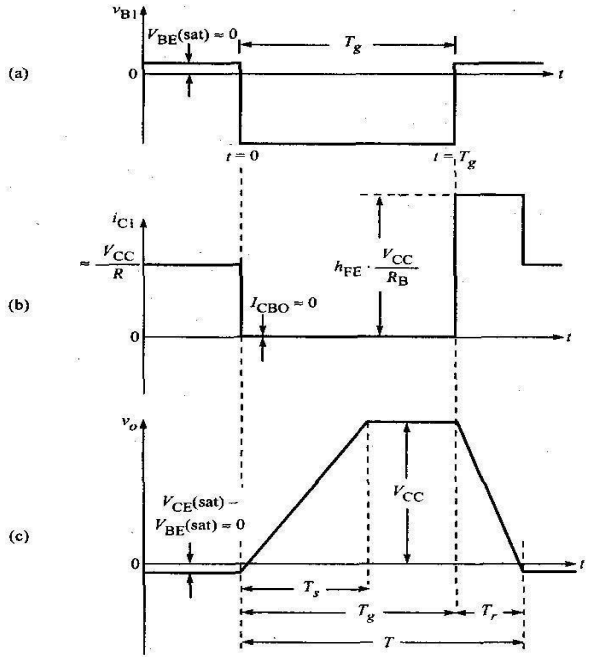


Fig.5.12 Voltage time-base generator of Figure 5.11: (a) the base voltage of Q1 (b) the collector current of Q1, and (c) the output voltage at the emitter of Q2

CURRENT TIME-BASE GENERATORS

We have mentioned earlier that a linear current time-base generator is one that provides an output current waveform a portion of which exhibits a linear variation with respect to time. This linearly varying current waveform can be generated by applying a linearly varying voltage waveform generated by a voltage time-base generator, across a resistor. Alternatively, a linearly varying current waveform can be generated by applying a constant voltage across an inductor. Linearly varying currents are required for magnetic deflection applications.

A SIMPLE CURRENT SWEEP

Figure 5.13 shows a simple transistor current sweep circuit. Here the transistor is used as a switch and the inductor *L* in series with the transistor is bridged across the supply voltage. *Rd* represents the sum of the diode forward resistance and the damping resistance. The gating waveform shown in Figure 5.26(b) applied to the base of the transistor is in two levels. These levels are selected such that when the input, is at the lower level the transistor is cut-off and when it is at the upper level the transistor Is in saturation. For $t < 0$, the input to the base is at its lower level (negative). So the transistor is cut-off. Hence no currents flow in the transistor and $iL = 0$ and VCE = Vcc- At f = 0, the gate signal goes to its upper level (positive). So the transistor conducts and goes into saturation. Hence the collector voltage falls to vCE(sat) and the entire supply voltage *Vcc* is applied across the inductor. So the current through the inductor

$$i_L = \frac{1}{L}\int V_{CC}\, dt = \frac{V_{CC}t}{L}$$

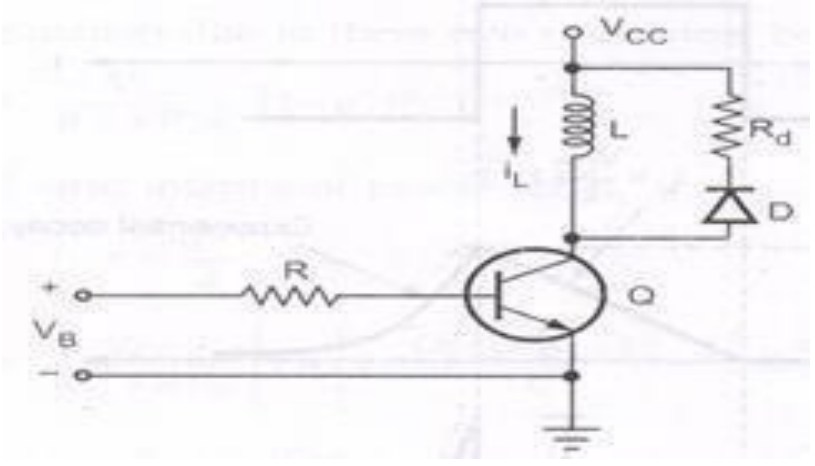


Fig.5.13 simple transistor current sweep circuit

Increases linearly with time. This continues till *t = Tg,* at which time the gating signal comes to its lower level and so the transistor will be cut-off. During the sweep interval *Ts* (i.e. from *t* = 0 to *t = Tg),* the diode D is reverse biased and hence it does not conduct. At *t ~ Ts,* when the transistor is cut-off and no current flows through it, since the current through the inductor cannot change instantaneously it flows through the diode and the diode conducts. Hence there will be a voltage drop of *lLRd* across the resistance *Rd.* So at *t = Tg,* the potential at the collector terminal rises abruptly to Vcc + *fiftd** ie - there is a voltage spike at the collector at *t = Tg.* The duration of the spike depends on the inductance of Z-^but the amplitude of the spike does not. For *t > Tg,* the inductor current decays exponentially to zero with a time constant *T- LIRd.* So the voltage at the collector also decays exponentially and settles at Vcc under steady-state conditions. The inductance *L* normally represents a physical yoke and its resistance *RL* may not be negligible. If *RCs* represents the collector saturation resistance of the transistor, the current increases in accordance with the equation

$$i_L = \frac{V_{CC}}{R_L + R_{CS}}(1 - e^{-(R_L+R_{CS})t/L})$$

$$\approx \frac{V_{CC}}{R_L + R_{CS}}\left(1 - \left\{1 - \frac{(R_L + R_{CS})t}{L} + \frac{1}{2}\left(-\frac{(R_L + R_{CS})t}{L}\right)^2\right\} + \dots\right)$$

$$= \frac{V_{CC}t}{L}\left(1 - \frac{1}{2}\frac{(R_L + R_{CS})t}{L}\right)$$

If the current increases linearly to a maximum value *IL,* the slope error is given by

$$e_s = \frac{I_L}{\frac{V_{CC}}{R_L + R_{CS}}} = \frac{(R_L + R_{CS})I_L}{V_{CC}}$$

A TRANSISTOR CURRENT TIME-BASE GENERATOR

Figure 5.14 shows the circuit diagram of a transistor current time-base generator. Transistor Q1 is a switch which serves the function of S . Transistor Q1 gets enough base drive from VCC1 through KB a °d hence is in saturation under quiescent conditions. At t = 0, when the gating signal is applied it turns off Q1 and a trapezoidal voltage waveform appears at the base of Q2. Transistors Q2 and Q3 are connected as darlington pair to increase the input impedance so that the trapezoidal waveform source is not loaded. Such loading would cause nonlinearity in the ramp part of the trapezoid. The emitter resistor *RE* introduces negative current feedback into the output stage and thereby improves the linearity with which the collector current responds to the base voltage. For best linearity it is necessary to make the emitter resistance as large as possible. *RE* is selected so that the voltage developed across it will be comparable to the supply voltage

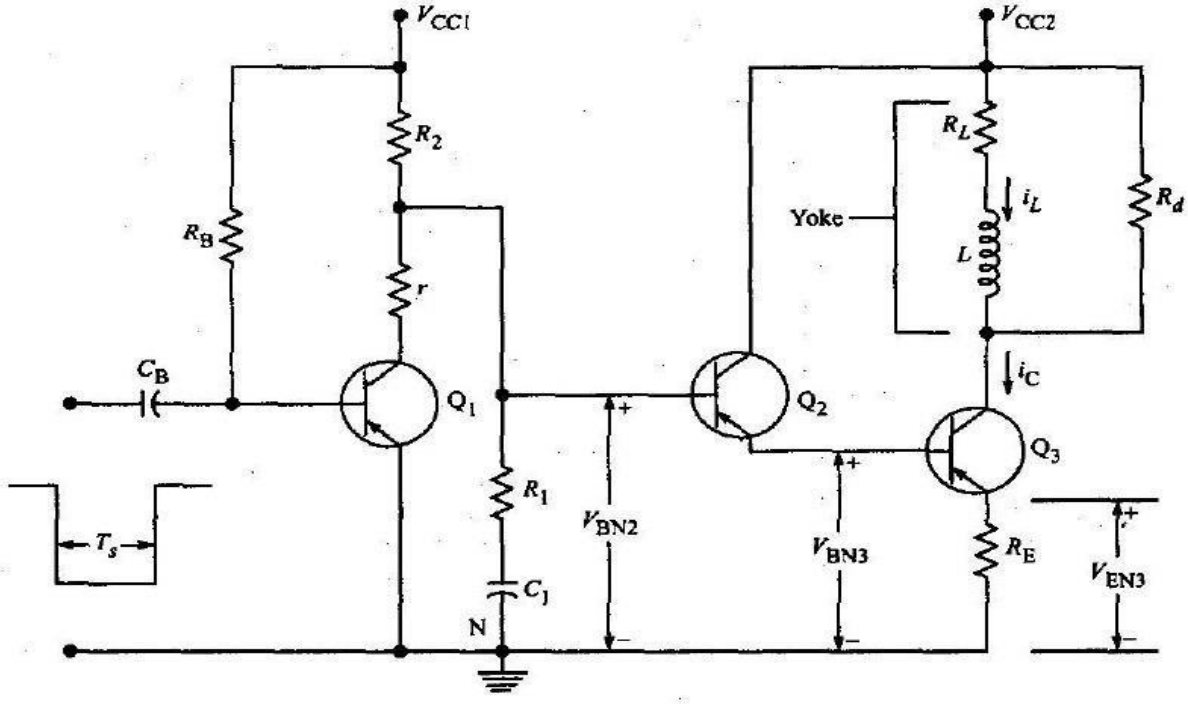


Fig.5.14 A Transistor Current Sweep Circuit

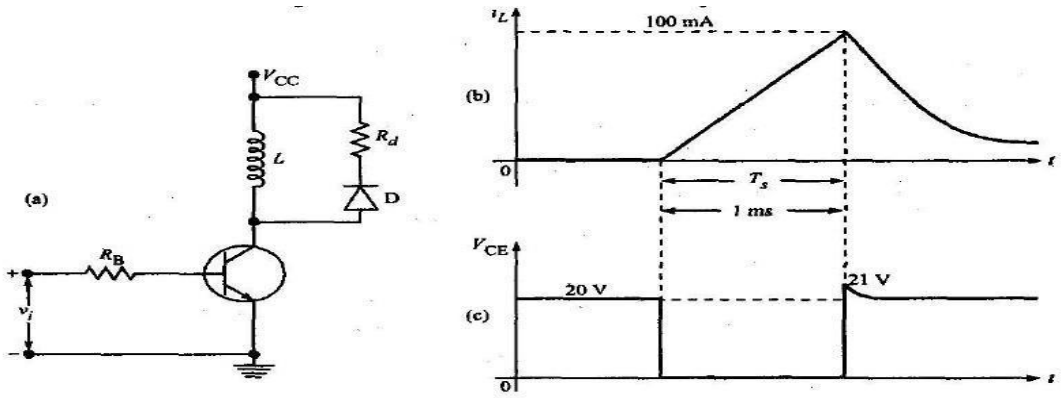


Fig.5.14 a) Circuit Diagram b) waveform of iL c) waveform of VCE

UNIT- V

Sampling gates.

Introduction :-

→ A Sampling gate is a transmission circuit in which the output is an exact reproduction of the input waveform during a selected time interval and is zero otherwise

→ Sampling gates are also called as linear gates because the output is exactly same as the input during the transmission interval

→ Sampling gates are also called as transmission gates or time selection circuits.

→ There are two types of Sampling gates
(i) Unidirectional Sampling gate
(ii) Bidirectional Sampling gate

→ Unidirectional Sampling gate is a Sampling gate which transmits Signal of only one polarity i.e either +ve or -ve

→ Bidirectional Sampling gate is a Sampling gate which can transmit Signals of both the polarities.

→ Sampling gates are different from the logic gates In logic gates there can be any numbers of inputs and outputs of the logic gates are either pulse or voltage levels and the output is not a reproduction of the input.

→ The output of a Sampling gate is an exact reproduction of input during the selected time interval.

→ The main applications of the Sampling gates are.

(i) Multiplexers
(ii) choppers
(iii) D/A converters
(iv) Sample and hold circuit.

→ Basic operating principles of Sampling gates :—

→ Sampling gates are uses Switches as diodes or transistors

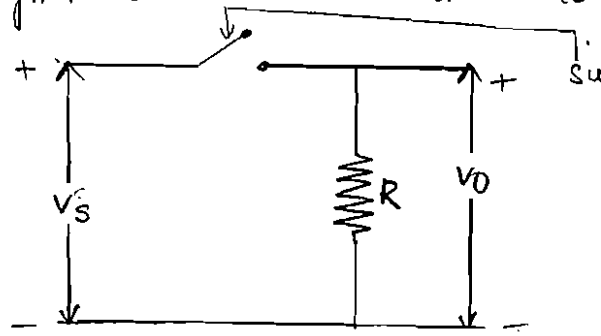
→ A Sampling gate using two types of switches circuits

(1). Series Switch

(2) Shunt Switch.

(1) A Sampling gate uses a Series Switch :— In which the input is inseries with a Switch. [either diode (or) transistor]

→ In this circuit, When the Switch is closed, then only input input Signal is transmitted to output. otherwise the input Signal is not transmitted to output. [i.e Switch is open]



Switch is operated by control Signal

→ When the Switch is open, then no voltage Signal will be appeared at the output

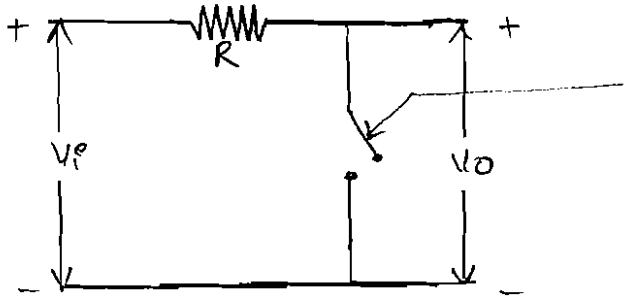
→ Operating of Switch is depends upon the control Signal.

(2) A Sampling gate uses a Shunt Switch :— Inwhich the input is inshunt With the Switch.

→ In this circuit, when the Switch is open, then only the input Signal is transmitted to the output, otherwise output voltage is zero.

→ When the switch is closed, then it is short circuit, so across the short circuit voltage is, zero, so $V_0 = 0$.

→ The equalent circuit for Sampling uses a Shunt Switch is Shown in below.



Switch is operated by control Signal

→ These Sampling gates uses Switches as Semiconductor devices like Diodes (or) transistors

→ When the device is conducting, it acts as a closed switch and when it is not conducting, it acts as a open switch.

→ Ideally, a closed Switch should have zero resistance and an open switch should have infinite resistance.

→ But Semiconductor devices do not have infinite back resistance and their forward resistances may lie in the range of several ohms.

→ When Such devices are used as Switches, there is no specific advantage of either the Series or the Shunt Switch position and the choice of the circuit is depends upon the particular application.

(I) Unidirectional Sampling gates :-

→ Unidirectional diode gates :-

A unidirectional diode gate can transmit either positive or negative pulses. to the output.

→ That means this gate transmits pulses of only one polarity to the output.

→ The input Signal is transmitted to the output only when the control Signal enables the gate circuit.

→ There are two types of unidirectional diode gates.

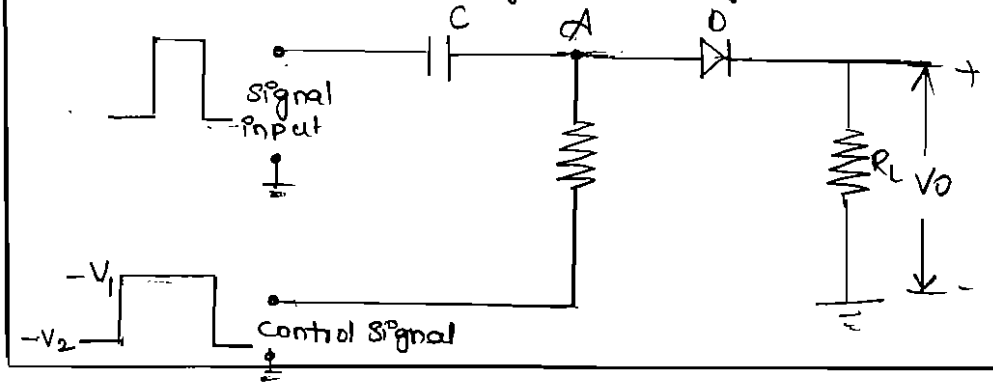
(i) Unidirectional diode gates that transmit positive pulses

(ii) unidirectional diode gates that transmit negative pulses.

→ (i) Unidirectional diode gates to transmit positive pulses :-

→ In order to transmit positive pulses, the unidirectional gate can be used.

→ If a control Signal is applied as negative Signal, then its magnitudes are changes abruptly between $-V_2$ and $-V_1$.



→ (i) When we are applying the control signal as $-V_1$, which is the large negative voltage value. then resultant voltage at the point A is negative.

→ Then the diode D will be off, because it requires a positive voltage to be conducting.

→ Now consider the duration, when the control signal has a value $-V_2$ (Smaller negative value) and the resultant voltage at A is some positive value. because at the point A, the input signal voltage value will be coincidence with control signal voltage value then resultant voltage value will be positive

→ Then diode D is ON. and whatever the input signal is applied that would be present at output, that can be taken across a load resistor (R_L).

→ For this the duration of control signal is large when compared to the input signal.

→ Let For example :—

Assume that the control signal has peak – peak value is 05 V. and the input signal has a peak – peak value will be 15V.

(i) $-V_1 = -40V$, $-V_2 = -15V$, and the input signal amplitude is 15V. $= V_i$

→ Then voltage at the point A is $V_A = ?$

Suppose we are applying control signal as $-V_1$.

then $V_A = -V_1 + V_i$.

$V_A = -40 + 15$

$\boxed{V_A = -25}$

→ At this voltage value, the diode D is off, then no output voltage i.e $\boxed{V_0 = 0}$.

→ Now we are applying control signal as $-V_2$.

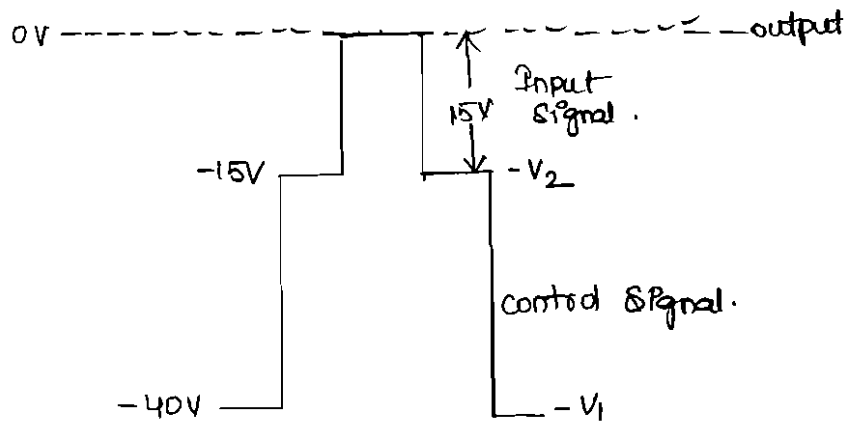
then $V_A = -V_2 + V_i$

$V_A = -15 + 15$

$\boxed{V_A = 0}$ → which is voltage at anode, which makes the diode D to be conducting

→ At this voltage value, the diode D is ON, then output will be present

→ It should be shown in below figure.



The control signal with $-V_1 = -40V$, $-V_2 = 15V$ and the input amplitude = 15V.

(ii) Now we are considered $-V_1$ as $-30V$, $-V_2$ as $-5V$. and the signal amplitude is 15V.

then voltage at A is $V_A = -V_1 + V_i$

$= -30 + 15$

$\boxed{V_A = -15}$

which makes the diode D into off, then no output voltage i.e $\boxed{V_0 = 0}$

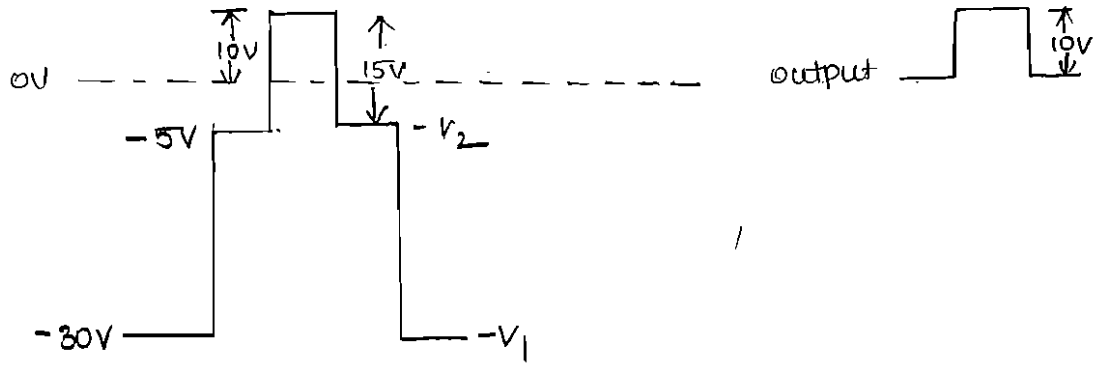
→ At the maximum level of control signal, we get the output i.e at $-V_2$.

then voltage at A is $V_A = -V_2 + V_i$

$= -5 + 15$

$\boxed{V_A = 10V}$

→ which makes the diode D into ON state, then output voltage will be shown in below figure.



The control signal with $-V_1 = -30V$, $-V_2 = -5V$, and the input amplitude = 15V.

(iii) Now we considered $-V_1 = -05V$, $-V_2 = 0V$ and the signal amplitude be 15V. ie $V_i = 15V$.

By applying $-V_2$, then voltage at point A is $V_A = 0+15 = 15V$.

→ This voltage makes the diode 'D' into ON state and the output will taken across R_L.

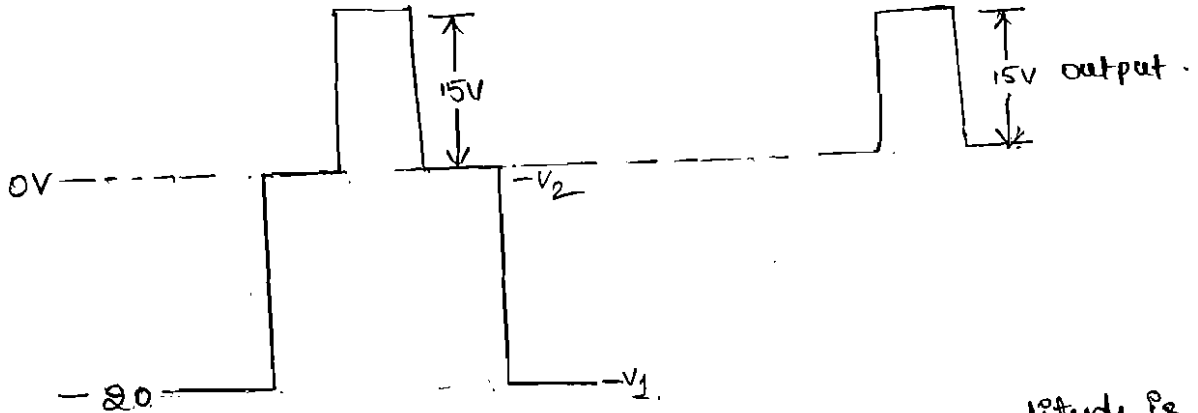
→ If we applying control signal value has $-V_1 = -25V$.

then voltage at point A is $V_A = -25+15$

$V_A = -10V$

→ This voltage makes the diode 'D' into off state

→ The output waveform is shown in below figure.



(iv) Let $-V_2 = 5V$, $-V_1 = -20V$, and the signal amplitude is $V_i = 15V$

→ By applying $-V_1$ as control signal value.

then voltage at point A is $V_A = -20+15$.

$V_A = -5V$.

→ which makes the diode 'D' into off state.

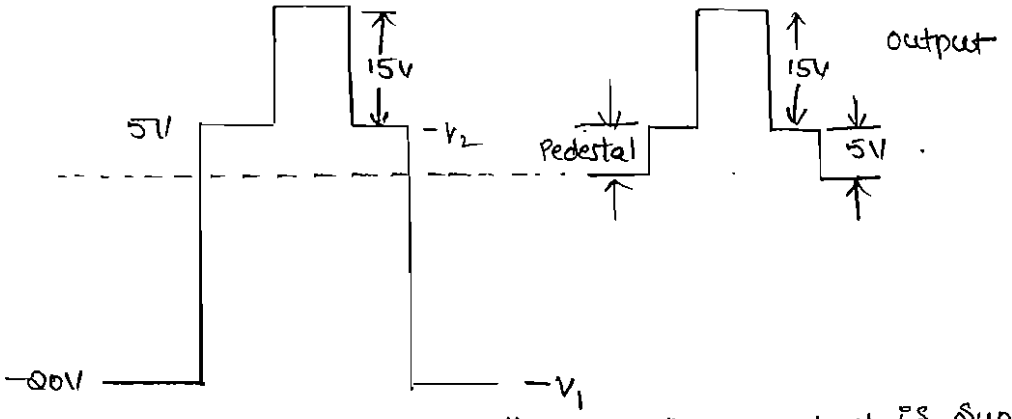
→ By applying $-V_2$ as control signal value.

then voltage at point A is $V_A = +2.5+15$.

$V_A = 20V$

→ which makes the diode 'D' into ON state and the output signal not only contains the input but also a position of the control signal.

→ The output waveform is shown in below figure

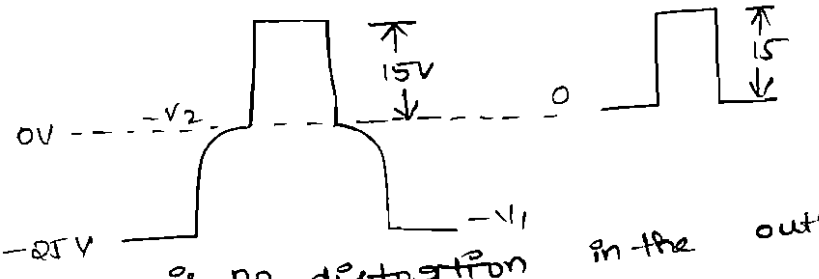


→ In the above case, it is seen that the output is superimposed on a pedestal of 5V. thus, the output is influenced by the control signal.

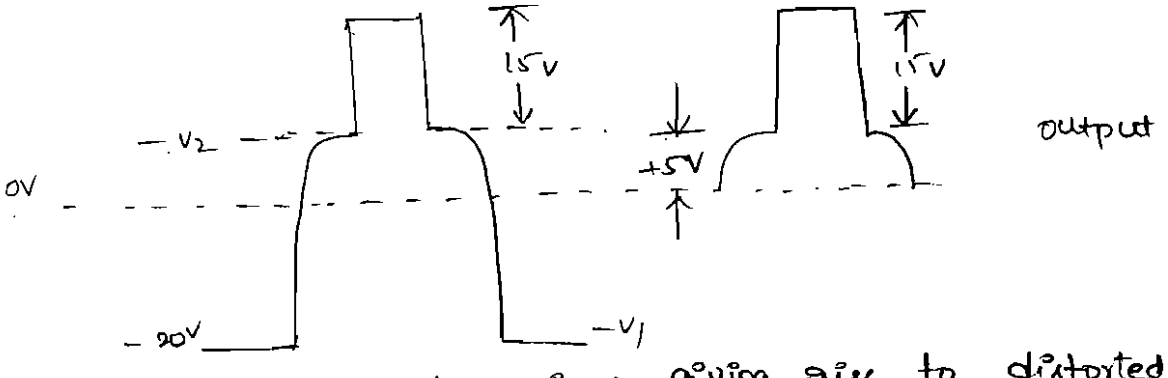
→ For a gating signal, RC network behaves as an integrator hence the gate signal (or) control signal is not necessarily a rectangular pulse. but rises and falls with a time constant RC. then distortion will be present at output.

→ Another reason for distortion is if the duration of the input signal is much greater than the duration of the control (or) gate signal.

→ The gating signal will have exponentially rising & falling edges as shown in below.



There is no distortion in the output though the control signal is distorted.



The distorted gate signal giving rise to distorted pedestal

→ Advantages of unidirectional diode gates:—

1. It is extremely simple
2. There is very little time delay through the gate
3. The gate draws no current in its quiescent condition
4. The control signal can be easily extended into a multi input OR circuit, with an INHIBITOR or NOT terminal

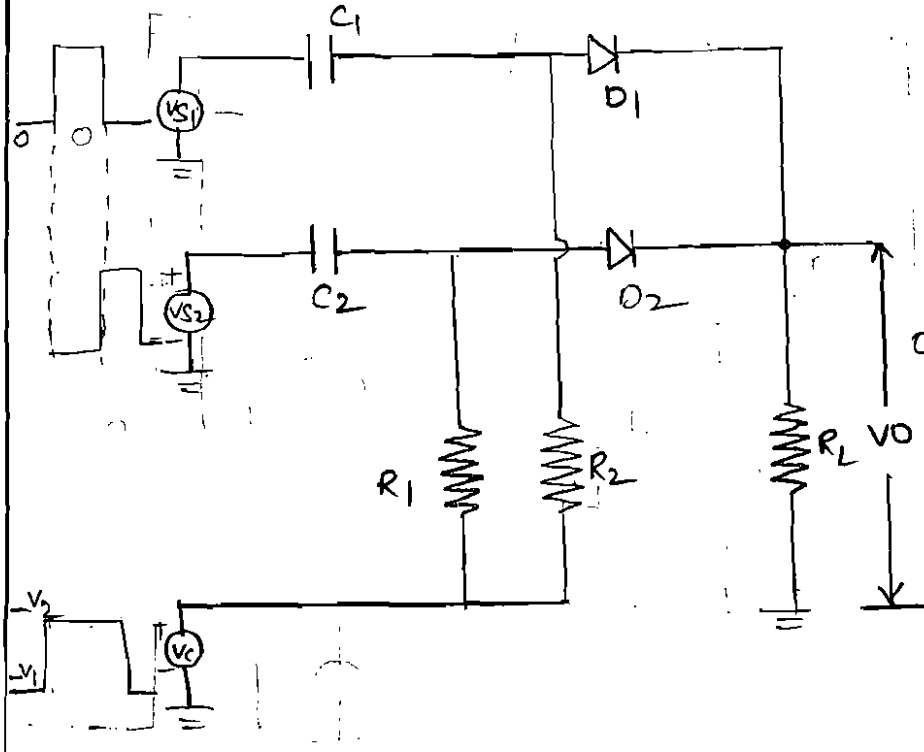
→ Disadvantages of unidirectional diode gates:—

1. There will be interaction between the signal source and the control voltage source
2. The control signal (gate) is of limited use because of the slow rise of the control voltage at the diode.

→ Unidirectional diode gates to accommodate more than one input signal:—

→ The below diagram shows the unidirectional diode sampling gate with two input signals.

→ But the signal can be extended to large number of inputs as well.

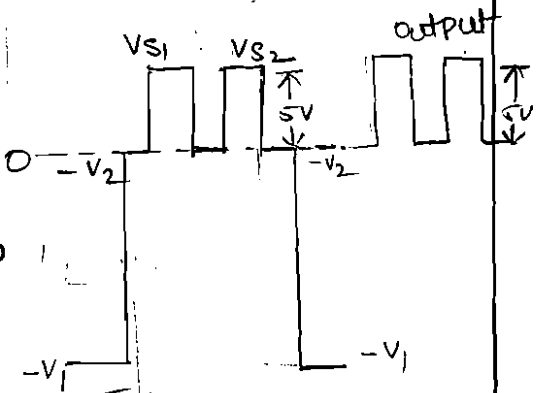


Output waveform

Let us consider $-V_1 = +2.5V$

$-V_2 = 0V$

$V_{S1} = V_{S2} = 5V$



→ i) When the control signal is at its lower level i.e $-V_1$ level [large -ve] then the diodes will be off, then no input signal can transmitted to the output.

→ ii) When the control signal is at its upper level i.e $-V_2$ level then the diodes will be ON. then output will be present

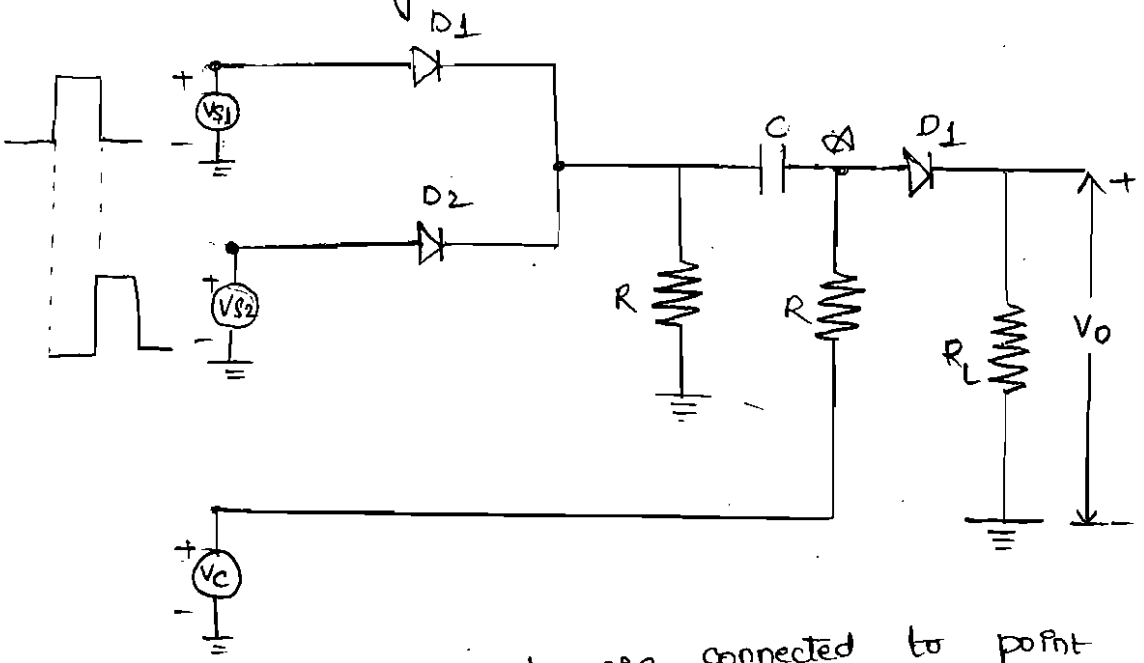
→ At that time, the control signal will acts as capacitively coupled - OR circuit. hence this negative level of the control pulse may be considered as an inhibitor signal.

→ so the circuit is called as multi - input OR circuit with an inhibition teaminal.

→ The drawback of this circuit is that the number of inputs increases, the loading on the control signal becomes excessively heavy.

→ To overcome this drawback, the circuit will be modified by using one more diode.

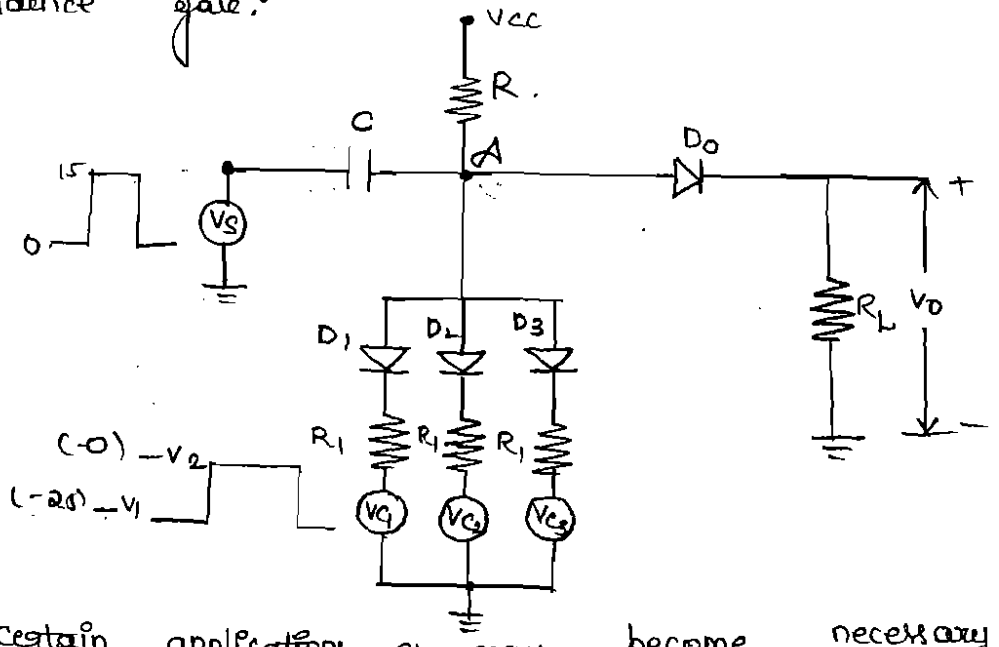
→ The below circuit arrangement avoids the loading on the control signal.



→ Here, the input signals are connected to point A through the diodes D_1 and D_2, whereas the control source is connected at A directly to avoid interference and the loading.

→ A unidirectional diode coincidence gate (or) A unidirectional diode AND gate :—

→ The below diagram shows the unidirectional diode coincidence gate.



→ In certain applications, it may become necessary that the input be transmitted to the output only when a set of conditions are simultaneously satisfied.

→ In such case, a coincidence gate is used.

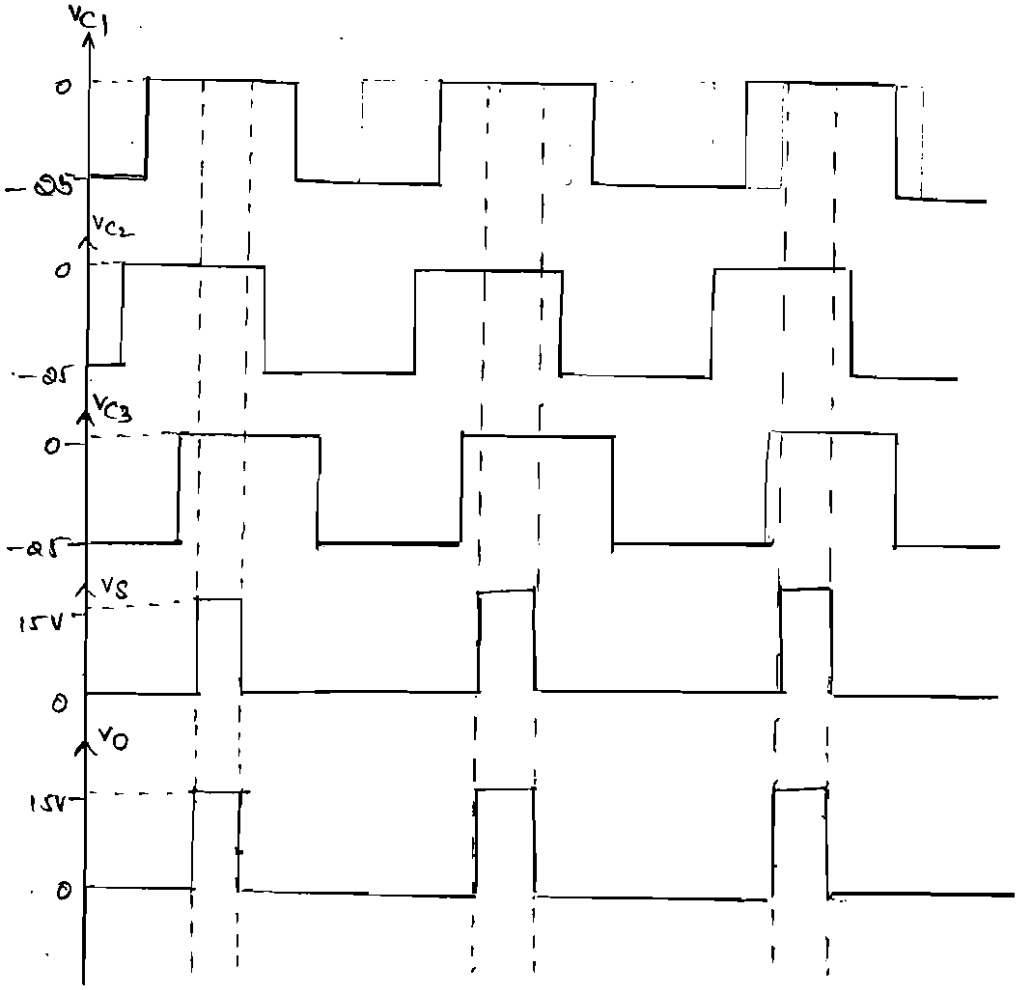
→ Let us considered, the control voltage values as $-V_1 = -25V$ $-V_2 = 0V$, & the amplitude of the given input signal as 15V.

→ Suppose we are applying control voltages at $-V_1$ level(-25) then potentials at point A at cathodes of three diodes (i.e D_1, D_2, D_3) will be '-ve'. then these three diodes are forward biased and then reached to the point A. which is the large -ve value

→ This large -ve value makes the diode 'D_0' into reverse biased, then it is open circuit. Hence there is no signal at the output.

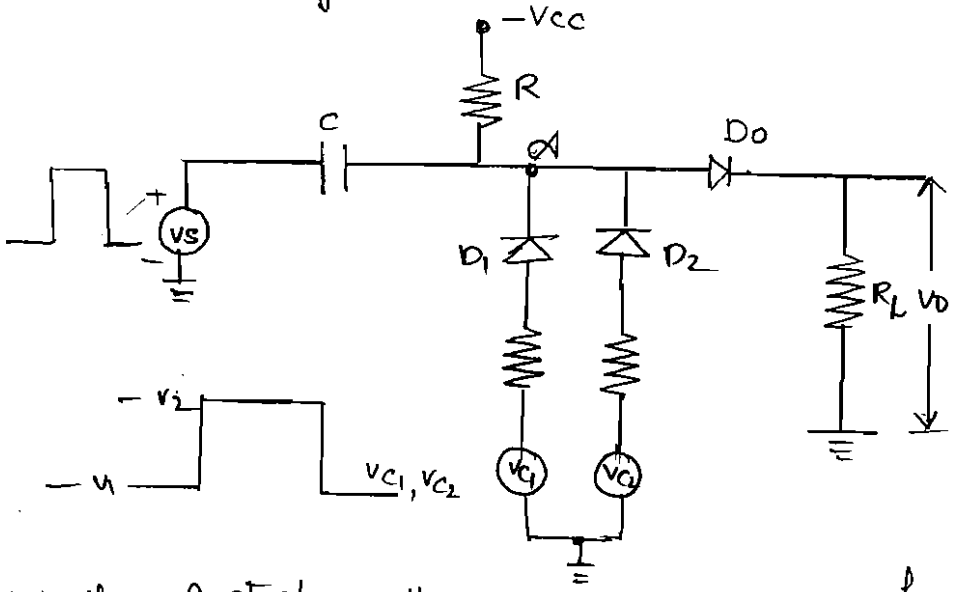
→ Similarly, when all the control voltages are at 0V, then those three diodes are reverse biased, then potential at point A is '+ve' value, because at that point the input signal is coincidence with it. then 'D_0' will be forward biased and the signal will be present at output.

→ The output waveform are shown in below figure.



→ A unidirectional diode OR gate:

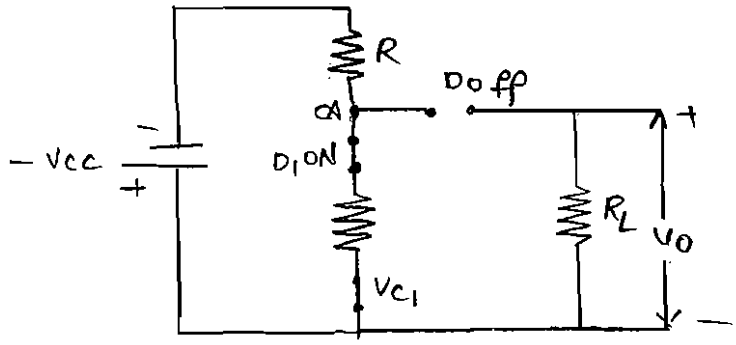
→ The below diagram shows the unidirectional diode OR gate.



→ Let the Control voltage values vary from $-V_1$ to $-V_2$

→ In two control signals, if any one of the control signal(V_{c_1}) at $-V_2$ level, then D_1 conducts and behaves as short circuit, hence Do is reverse biased and is an open circuit

→ Then the resultant circuit is shown in below.



→ Because of D0 is reverse biased, the output value is zero.

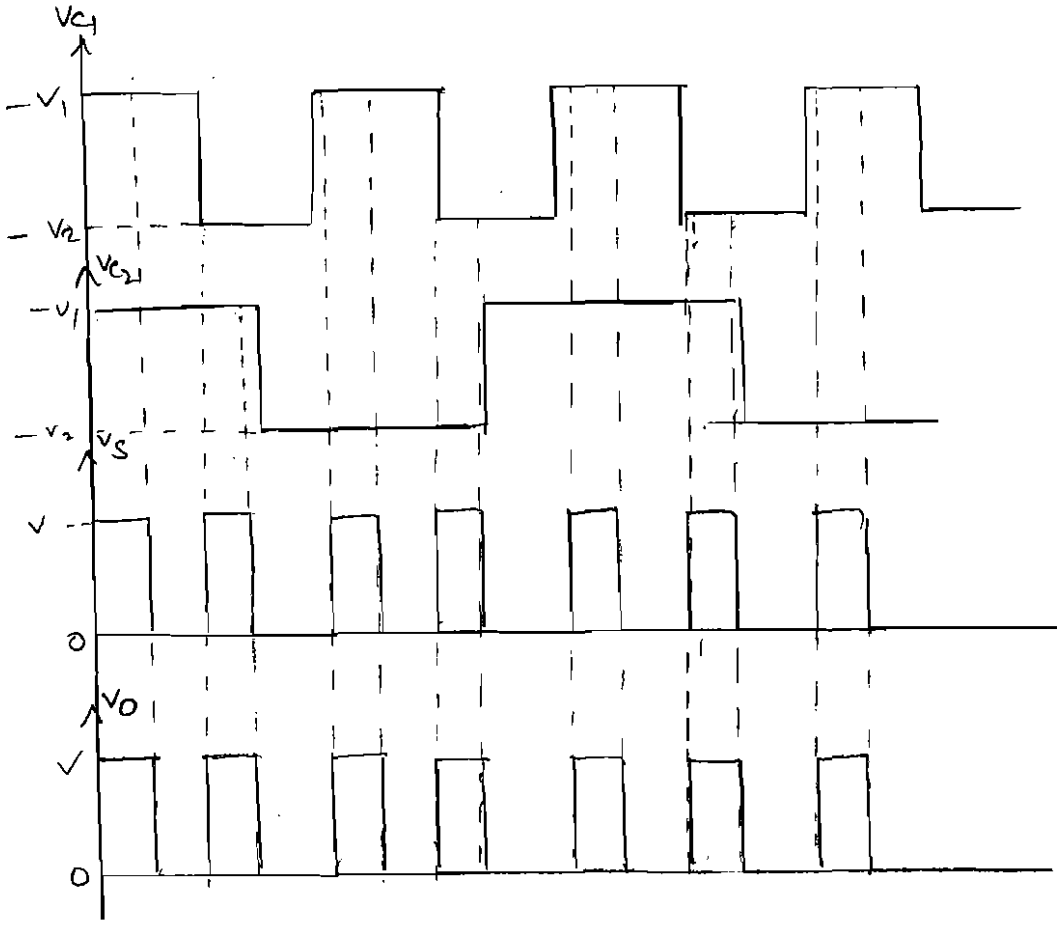
→ If the second level of control signal is applied i.e $-V_1$ then the two diodes will be off, then whatever input voltage applied that would be present at point A, which makes the diode D0 into ON state.

→ then input is transmitted to the output

→ From this it is clear that, any one of the control signal is low then only we get the output.

→ So this circuit is called as an OR circuit.

Output waveform:-



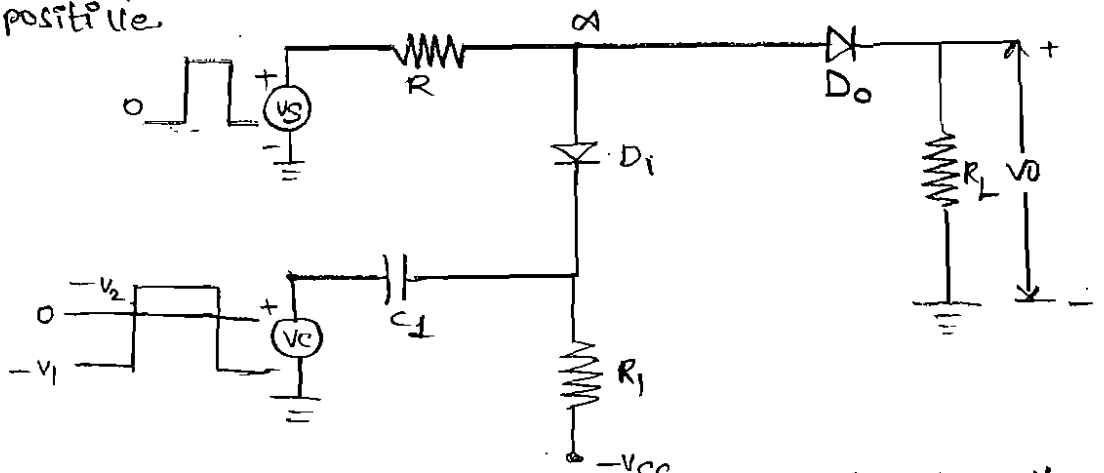
→ Unidirectional diode gate that eliminates pedestal :—

→ upto now, We are seen that, the unidirectional diode gates will gives the output only at the upper level of the gating signal is exactly equals to zero volts.

→ then control signal enabled and an input is faithfully transmitted to the output

→ If the control signal has upper level as some positive voltage, then We get pedestal at the output.

→ By using following circuit, we get faithful replica of the input even if the upper level of control signal is positive.



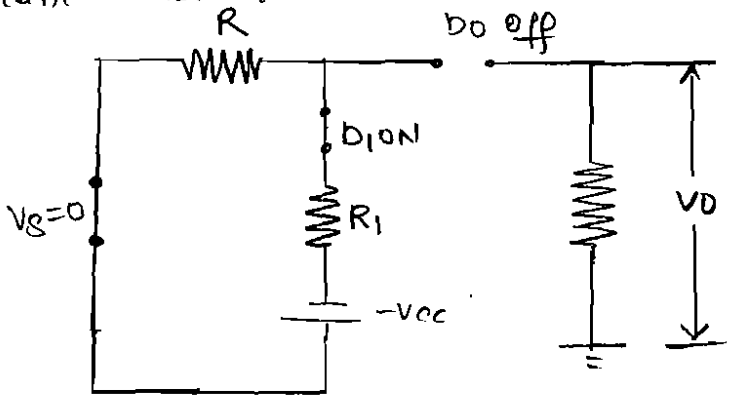
A Sampling gate that is insensitive to the upper levels of the control signal.

case(i) :—

If the input V_s is zero and if the control signal is not present. then D_1 is conducted by using $-V_{cc}$ supply which is connected to the cathode of diode D_1, which makes the diode D_1 into ON state.

→ Then resultant voltage at point A is '−ve' value this voltage makes the diode 'D_o' into off state.

→ The resultant circuit is shown in below



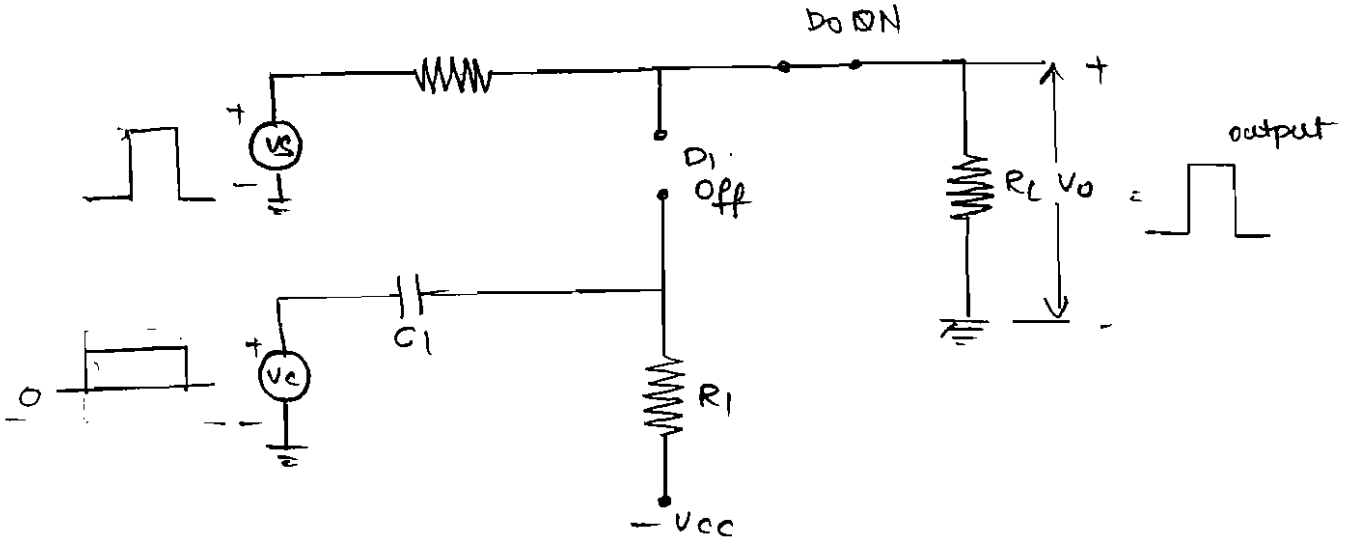
case (ii) :—

If the control voltage is now positive, and input signal is also applied, then the diode D_1 will be reverse biased.

→ then potential at point A is positive because it is coincidence with input signal.

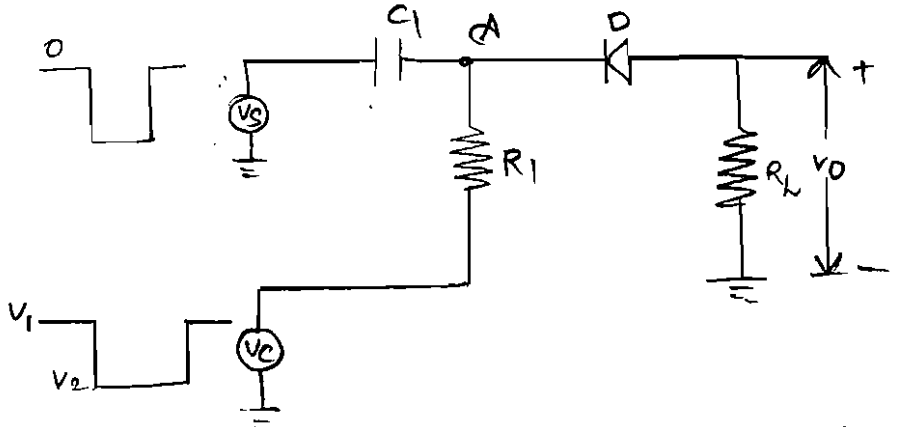
→ This positive voltage makes the diode 'D' into ON state then it is short circuit, then input will be transmitted to output without any pedestal.

→ The equalent circuit is shown in below.



2) A unidirectional diode gate to transmit negative pulses :—

→ The below diagram shows the unidirectional diode gate to transmit negative pulses.



→ In this circuit, the differences are when compared to previous circuits is that the two signals, input signals are negative pulses and the control signal varies between V_1 and V_2. and the diode is connected in the opposite direction.

i) The control signal is at V_1 which is the large positive value then resultant voltage at point A is positive.

→ then the diode D will be off. then no input signal will be transmitted to the output

ii) Now the control signal is at V_2 level which is the small positive value then resultant voltage A is -ve value because at that point -ve input signal will be coincident

→ so this negative voltage makes the diode 'D' into ON state.

Output waveform:-

→ let us assume the peak-peak control voltage value as 20V. and the amplitude of input signal is -15V.

→ let us consider, $V_1 = 20$, $V_2 = 5$, amplitude of input signal is -15V

→ If apply the V_1 as control signal, then voltage at point A is.

$$V_A = 20 - 15 = 5.$$

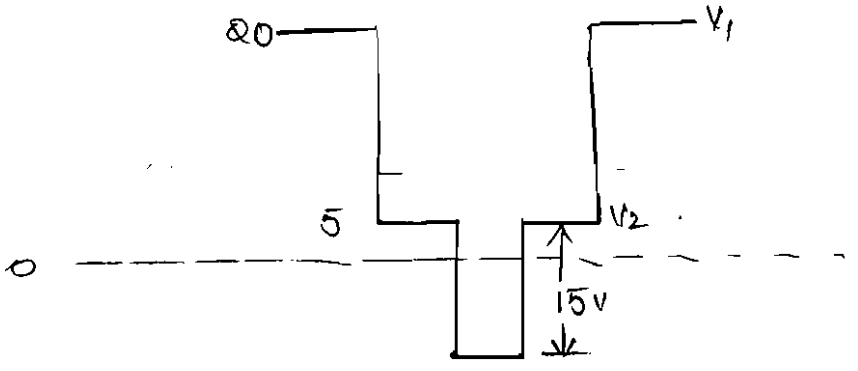
→ this voltage makes the diode D into off state.

→ and later apply control signal at V_2 level then resultant potential at point A is.

$$V_A = 5 - 15 = -10\,V$$

→ This negative voltage will makes the diode D into ON state.

→ the output waveform is shown in below figure.



Bidirectional Sampling gates :—

→ Bidirectional Sampling gate is a Sampling gate which transmit Signals of both the polarities.

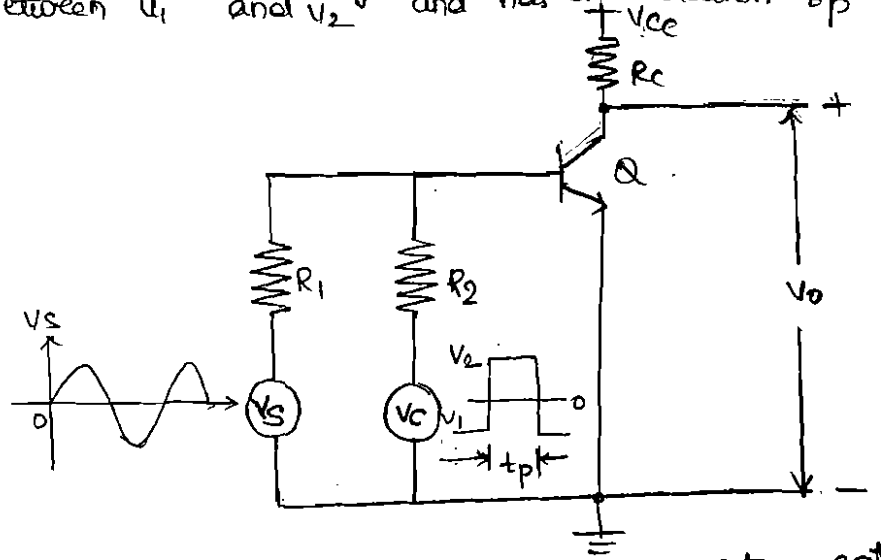
→ These gates are using diodes, BJTs, FETs etc.

→ we are going to consider the some variations of the bidirectional gates.

Single transistor bidirectional Sampling gates :—

→ The below diagram shows the single transistor bidirectional Sampling gate.

→ The control Signal is a pulse whose amplitude is varied between V_1 and V_2 and has a duration t_p sufficient enough for a Signal transmission



A bidirectional transistor gate.

→ Working of the transistor :—

→ If we applying control Signal at V_1 $(-ve)$ and the input Signal will be applied to the base of the transistor. then the transistor Q will be cutt-off because of the negative potential.

→ Then output voltage is Vcc. i.e $\boxed{V_o = V_{cc}}$

→ And later, apply the second level of control Signal i.e V_2 $(+ve)$ and it is combined with input Signal will be applied at base of the transistor which makes the transistor into ON state, then Current I_c will be passing through resistor Rc then $\boxed{V_o = V_{cc}}$

→ Then the input Signal is Succesfully amplified by the transistor, and transmitted to the output with phase inversion [The transistor provides 180° phase shift]

→ The input will be transmitted to the output during transmission period of control Signal only [i.e t_p]

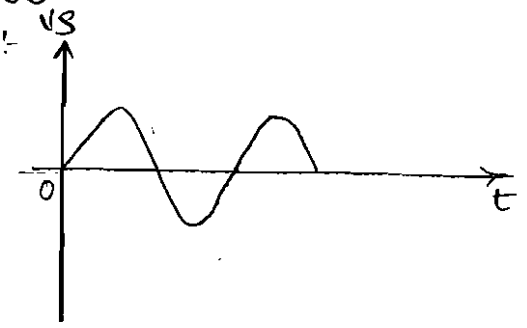
→ At the end of tp, Q is again off and its output voltage will jumps to Vcc.

→ Thus the signal is transmitted when the gating signal at V_2.

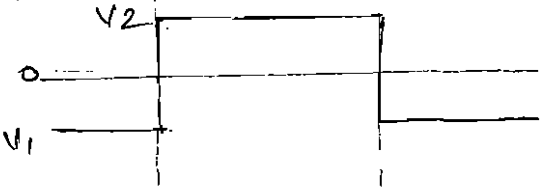
→ However the output contains a pedestal. (i.e reference level)

Output Waveform:-

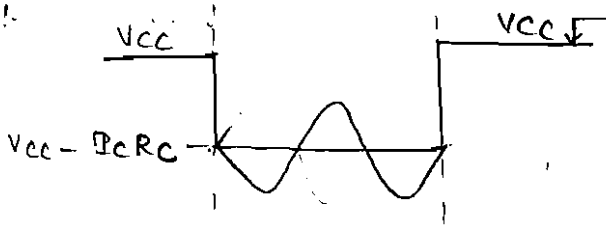
Input signal:-



Control Signal:-



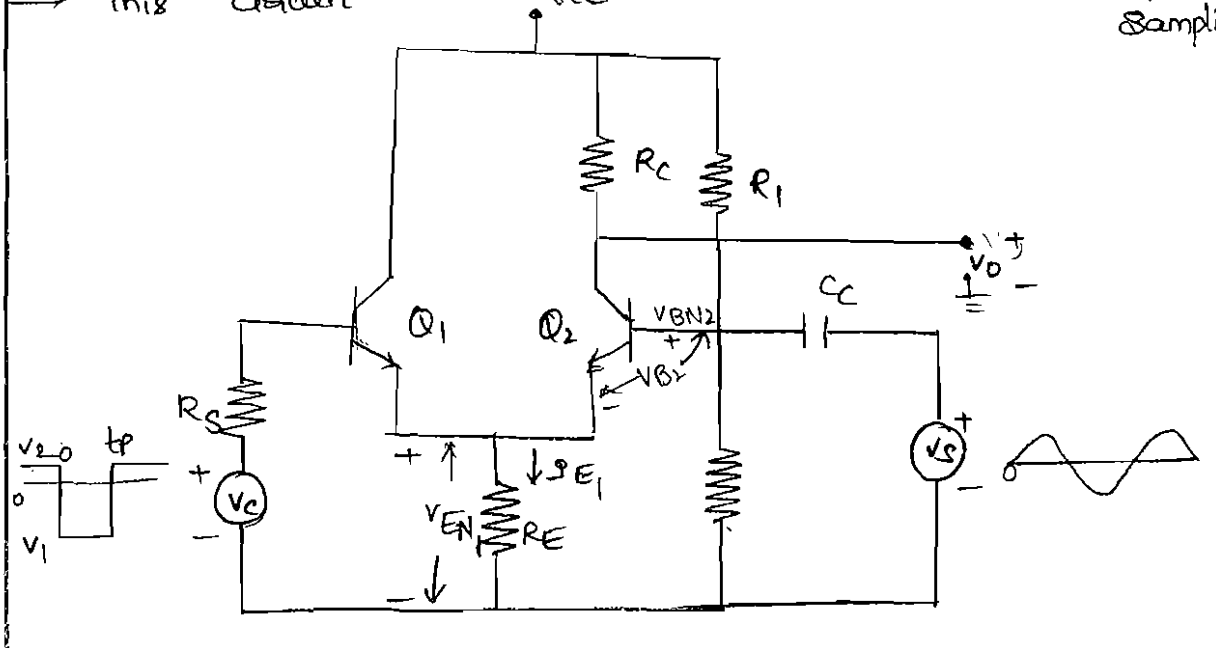
output:-



→ Two transistors Bidirectional Sampling gate:-

→ The below diagram shows the bidirectional sampling gate with two transistors.

→ This circuit is also called as emitter coupled bidirectional sampling gate.



→ In this circuit, the control signal and the input signal are connected to two seperate bases.

→ When the control signal at its upper level V_2 will be applied at the base of the transistor Q_1, (+ve) then transistor Q_1 will be ON, then high amount of current will be passed through collector and then emitter current will be increases i.e (I_{E_1}) then drop across the resistor R_E will be increased. [i.e V_{EN_1}].

→ This increased droping voltage will makes the transistor Q_2 into (off) state. because the two emitters of transistors are connected together.

→ Then output voltage is taken across the collector of the second transistor Q_2. then output must be equals to V_{cc}.

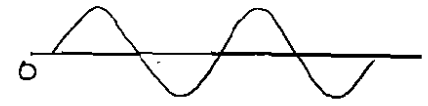
→ The equation $\boxed{V_o = V_{cc}}$

→ when the lower level of control signal is applied ie V_1 then which is the -ve value, which makes the transistor Q_1 into off state.

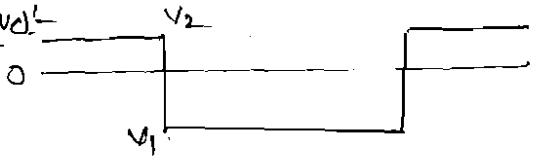
→ Q_2 is biased to operate in the active region using R_1 and R_2 then the input signal is connected to the base of the Q_2, so it will be appeared at the output with phase inversion.

→ At the end of the gating signal then $V_o = V_{cc} - I_{c_2}R_c$ and Q_2 goes into off and V_o jumps to V_{cc} output waveforms Hence the signal is superimposed on pedestal

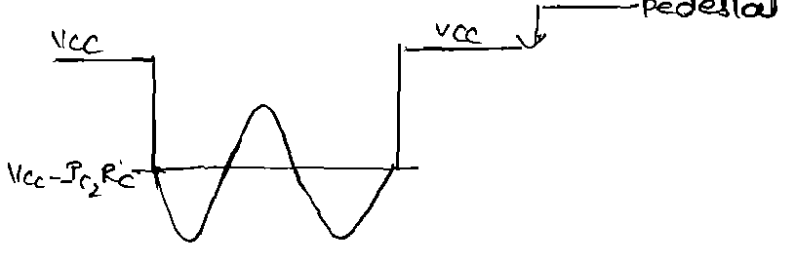
Input Signal(V_s):-



Control signal(V_c):-



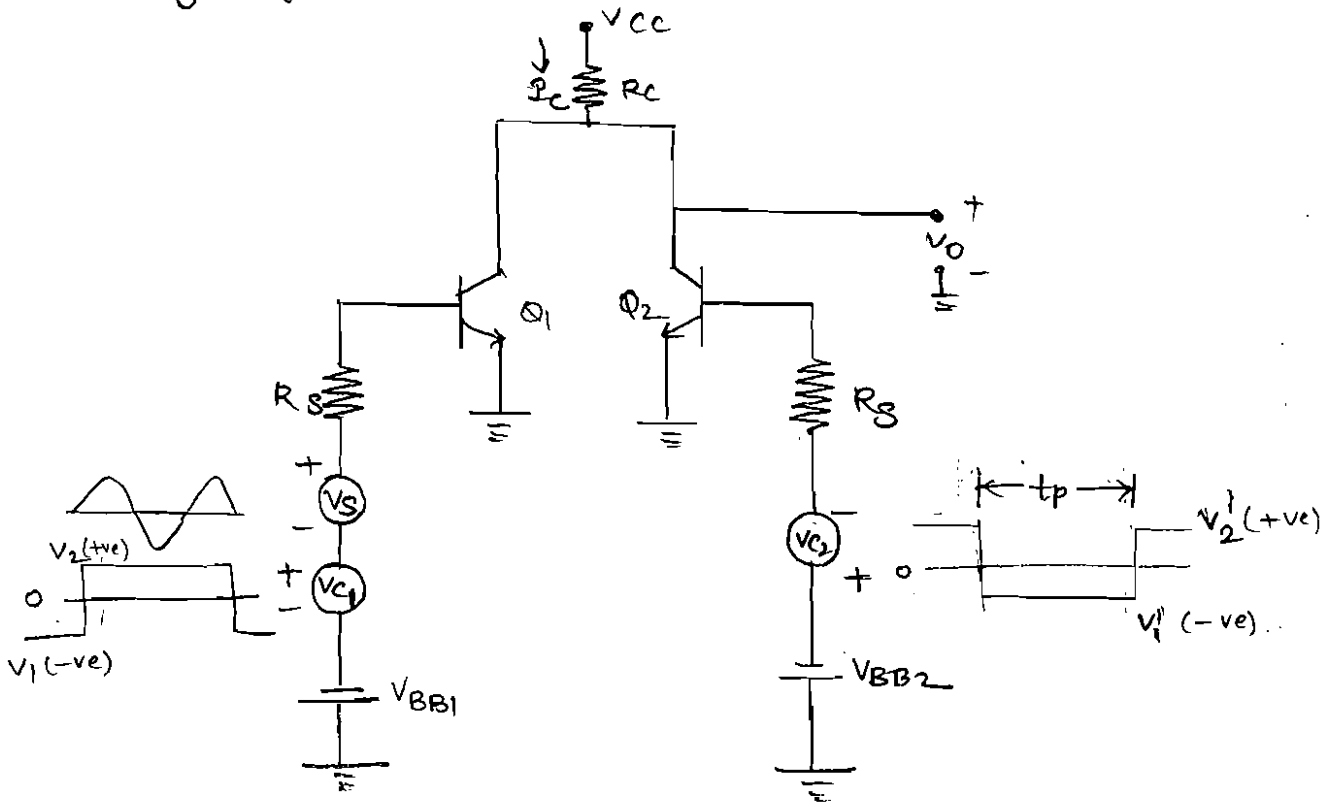
output:-



→ A two transistor bidirectional Sampling gate that reduces the pedestal :—

→ In above two topics, we are seen that pedestal will be appeared at the output, that can be overcomed by using the following circuit.

→ Which is also called as collector coupled bidirectional Sampling gate.



Working :—

→ These two control signals have the same amplitude with opposite polarities will be applied to this circuit

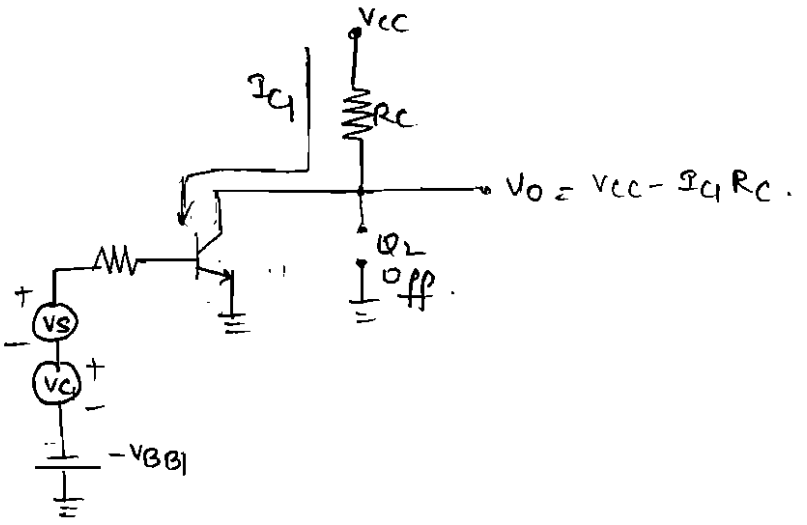
→ When control signal V_{C_1} at its upper level V_2 (+ve) is applied at the base of the transistor Q_1 and as well as the control signal V_{C_2} has to be applied V_1' (−ve) value will be applied at the base of the transistor Q_2

→ Because of this control voltages, the transistor Q_1 will be ON and the transistor Q_2 will be off.

→ Then from Vcc, the current will be passed through an resistor Rc [i.e I_{C_1}] to a transistor Q_1 because it is in active region. no current will be passed to Q_2 because it is open

→ So the output is taken across the collector of the transistor Q_1. with an amplified version during transmission period only.

→ The equalent circuit is shown in below.



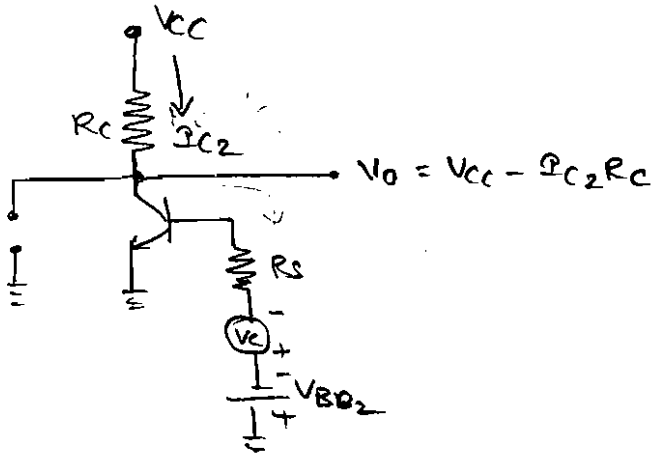
→ And then, the control signal V_{C_1} of second level V_2 (-ve) value will be applied at the base of the transistor Q_1. and as well as control signal V_{C_2} of second level. V_2' (+ve) will be applied at the base of the transistor Q_2 this +ve voltage makes the transistor Q_2 into ON state and Q_1 will be off because of -ve voltage

→ So the collector of second transistor will draws a current I_{C_2} through R_C.

→ output voltage is taken across the collector of transistor Q_2.

i,e $\boxed{V_o = V_{cc} - I_{C_2} R_C}$

→ The equalent circuit is shown in below.

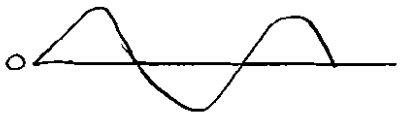


→ these the input signal is not proportional to output, because it is connected to the base of the transistor Q_1

→ In output these is no pedestal, and the currents I_{C_1} & I_{C_2} will be same, because the same amplitudes of control signals will be used with opposite polarity

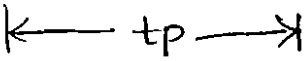
output Waveforms:-

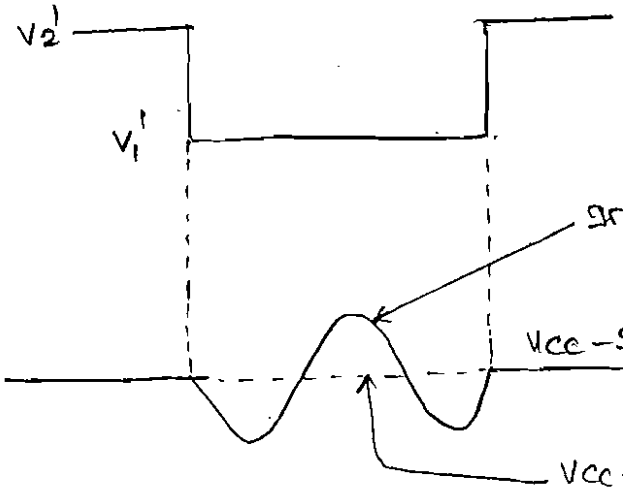
Input Signal (Vs):-



control Signal (V_{C1}):-

control Signal (V_{C2}):-





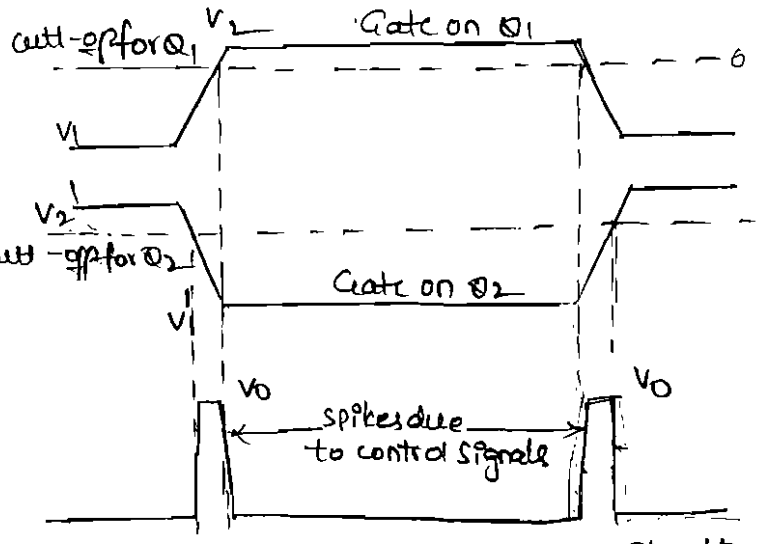
output:-

→ This ciacuit did not solve the paoblem of pedeital, the control Signals will have non zero aise time & fall time.

→ The gated Signal (control Signal) aise time is small compaied with the control Signal, the Spike will be paesent at the output.

→ Because of this aising and falling edges of control Signals both the tranaistoas will be cutt-off, then output reaches to Vcc. It will be the daaw backs of this ciacuit

→ It will be shown in below waveforms.



→ The spikes of longer duration if the rise time of the gating signal is large.

→ The circuit of used to eliminate pedestal has the following drawbacks:-

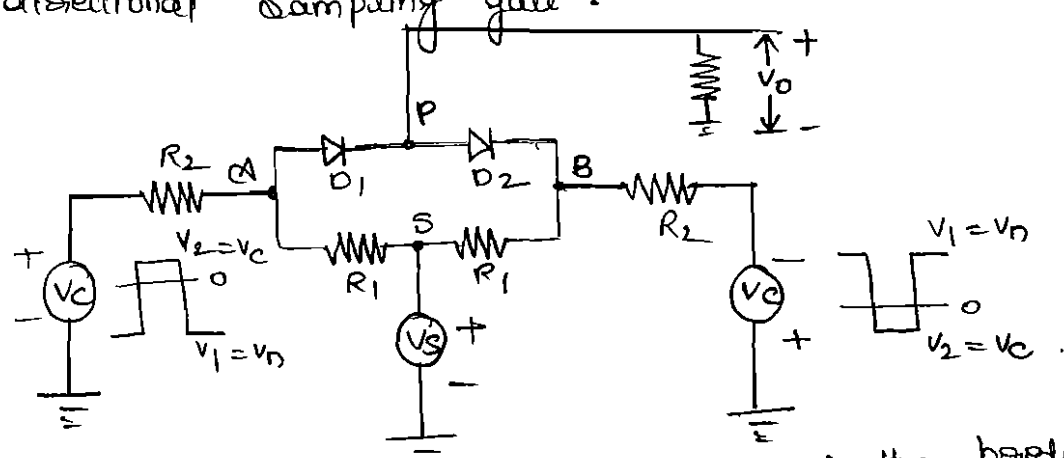
1) If the gating waveform have definite rise and fall times two sharp spikes are generated at the output.

2) There is a continuous flow of current through R_C and so it has to dissipate a lot of heat.

3) The circuit is complicated. It requires two bias voltages i.e $-V_{BB1}$ and $-V_{BB2}$ and two control signal sources which are complements of each other.

→ Two diode bridge type bidirectional sampling gate that eliminates the pedestal (or) Bidirectional diode sampling gate:-

→ The below diagram shows the two diode bridge type bidirectional sampling gate.



→ these R_1, R_1 D_1 & D_2 form the four arms of the bridge.

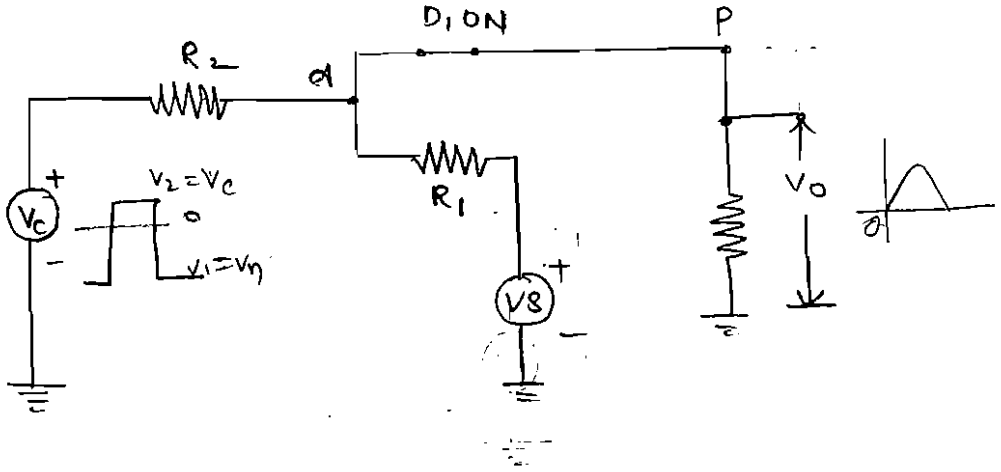
Working:-

(i) When the control signal at level V1 [i.e +Vc] is applied to the diode D_1 with positive input cycle.
and the second control signal at level V2 [$-V_c$] is applied to the diode D_2.

→ Then D_1 will be ON with positive going signal and D_2 will be off.

→ So the output voltage is positive half cycle.

→ The equalent circuit is shown in below.



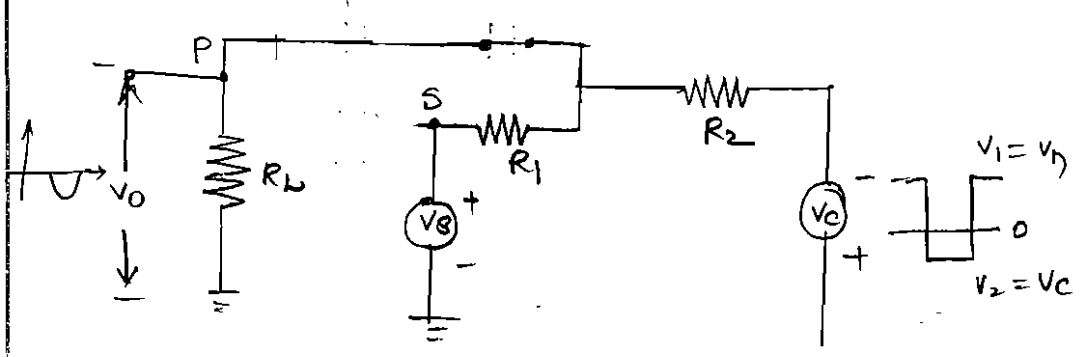
(ii) When the control signals are at V_2 levels ie $+V_n$ is connected to the diode D_2 and $-V_n$ is connected to the the diode. ~~input voltage is~~ ~~the half cycle~~.

→ then both the diodes will be off.

(iii) when the control signal at V_2 level $(-V_c)$ is applied to the diode D_2 with -ve half cycle. the D_2 will be ON & D_1 will be off.

→ So the negative half cycle will transmitted to the output through the diode D_2.

→ The equalent circuit is shown in below.

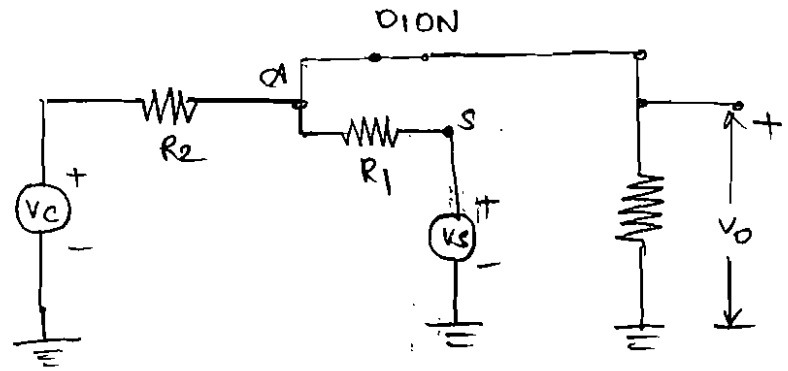


→ So the input signal is transmitted to the output sucessfully but it could not occur simulataneously.

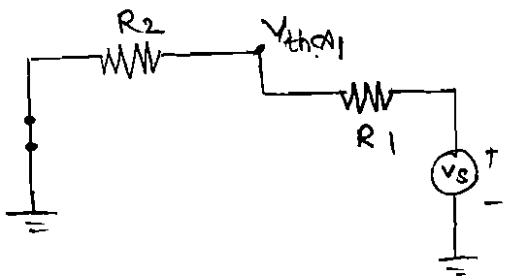
→ keeping the both the diodes into ON state for getting both +ve & -ve half ~~half~~ cycles simulalaneously, to calculate some Vc (min) voltage.

→ for this analysis we have to convert the circuit into thevinizing circuit.

Consider the circuit transmits the positive pulses to the output



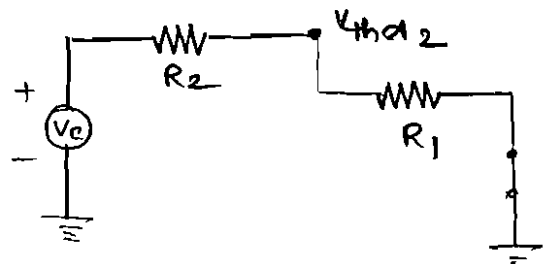
→ Thevenin voltage source magnitude due to Vs (shorting Vc source) considering one source at a time).



$$V_{th@1} = V_S \times \frac{R_2}{R_1+R_2}$$

→ considered $\frac{R_2}{R_1+R_2}$ as α.

then $V_{th@1} = V_S \alpha$ ——→ (1).



$$V_{th@2} = V_C \frac{R_1}{R_1+R_2}$$

$$V_{th\alpha_2} = V_S \frac{R_1}{R_1+R_2}$$

$$V_{th\alpha_2} = V_S[1-\alpha] \rightarrow (2).$$

$\left[\because \alpha = \frac{R_2}{R_1+R_2}\right.$

$1-\alpha = 1-\frac{R_2}{R_1+R_2}$

$= \frac{R_1+R_2-R_2}{R_1+R_2}$

$\left.1-\alpha = \frac{R_1}{R_1+R_2}\right]$

the resultant thevenins voltage is

$$V_{th\alpha} = V_{th\alpha_1} + V_{th\alpha_2}$$

$$V_{th\alpha} = \alpha V_S + V_C[1-\alpha] \rightarrow (3).$$

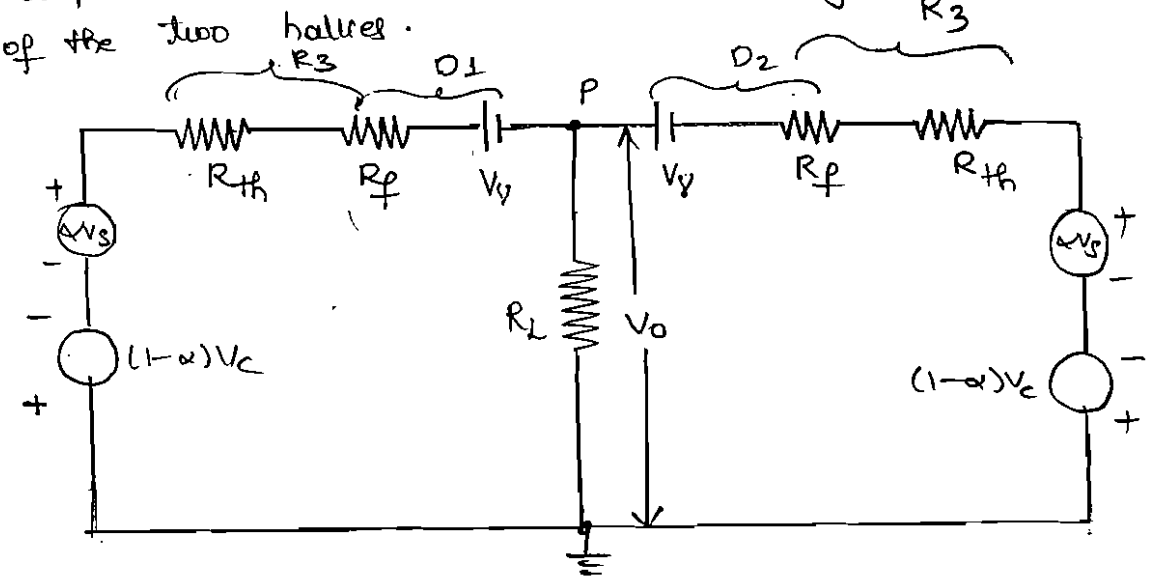
→ Thevenens resistance R_{th} is

$$R_{th} = R_1 // R_2$$

$$R_{th} = \frac{R_1 R_2}{R_1+R_2}$$

→ Replacing Redrawing the circuit with thevenens voltage & resistance and replace the diode with cutt-in voltage V_γ and the forward resistance R_f. Here the diodes are replaced by piecewise linear model.

→ similarly considering the circuit when a negative signal is transmitted to the output when D_2 is ON and combining the equalent circuits of the two halves.

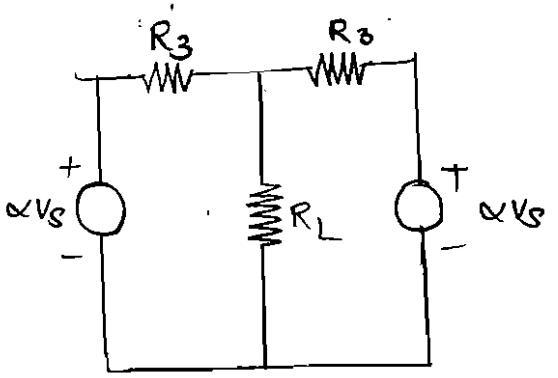


→ From the above circuit, we can observe that offset voltages V_γ and V_γ and the control voltage components $(1-\alpha)V_c$ tary to send equal current in opposite direction on R_L and hence the net current due to them is zero.

→ The open circuit voltage at p with respect to ground is αV_S (because all the sources are neglected)

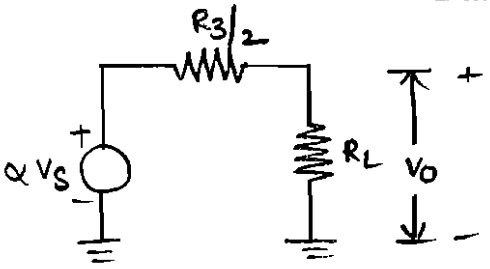
→ And the thevenin's equalent resistance at P with respect to ground is $R_3/2$

→ The circuit is simplified as follows.



Simplified circuit

→ The circuit that enables the calculation of gain A.



$$V_O = \alpha V_S \times \frac{R_L}{R_L + R_3/2}$$

We know that gain $A = \frac{V_O}{V_S}$

$$= \frac{\alpha V_S \times \frac{R_L}{R_L + R_3/2}}{V_S}$$

$$= \frac{\alpha V_S}{V_S}\left[\frac{R_L}{R_L + R_3/2}\right]$$

$$A = \alpha \cdot \left[\frac{R_L}{R_L + R_3/2}\right]$$

we know that $\alpha = \frac{R_2}{R_1 + R_2}$

Substitute this value in above equation

then $$\boxed{A = \left[\frac{R_2}{R_1 + R_2}\right]\left[\frac{R_L}{R_L + R_3/2}\right]}$$

1) Minimum control voltage $V_{c(min)}$ required to keep both the diodes D_1 and D_2 ON?

→ Let only the gating signals be present. the amplitude and polarity of the gating signals are such that both the diodes D_1 and D_2 conduct, and equal currents flow in these two diodes. when these equal & opposite currents flow in R_L, the net voltage drop is zero and there is no pedestal.

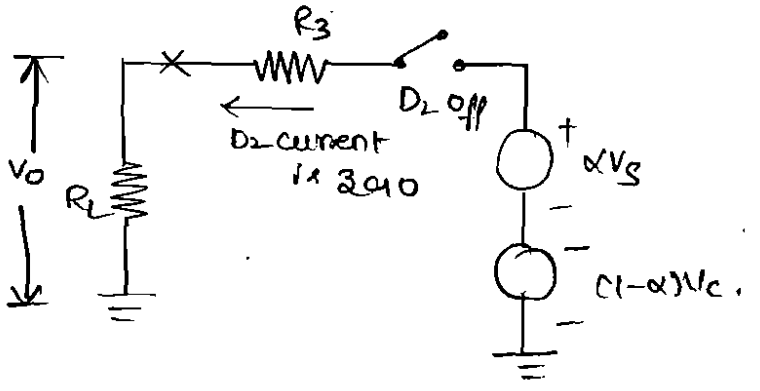
→ let V_s be the positive signal. As the amplitude of the signal goes on increasing the current in D_1 goes on increasing and that in D_2 goes on decreasing.

→ As V_s increasing further, the current in D_2 becomes zero. (i.e D_2 off).

→ That there is minimum control voltage V_c that will keep both the diodes ON.

→ To calculate this $V_{c(min)}$ let it be assumed that D_2 has just stopped conducting. i.e the diode current has become zero. the drop across R_3 is zero. therefore, the output voltage across R_L is the open voltage.

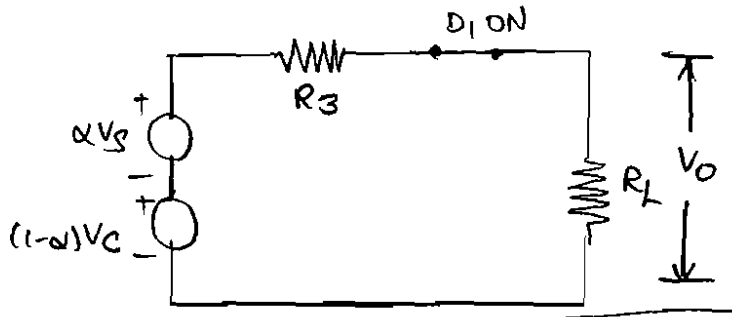
→ The equalent circuit is shown in below figure



→ The voltage V_o, when D_2 is off. in parallel voltage is same

so $\boxed{V_o = \alpha V_s - (1-\alpha)V_c} \rightarrow (4)$

→ when D_1 is ON, the equalent circuit is shown in below



the output voltage $\boxed{V_o = [\alpha V_s + (1-\alpha)V_c]}$ $\rightarrow (5)$ $\boxed{V_o = [\alpha V_s + (1-\alpha)V_c]\frac{R_L}{R_L+R_3}}$

→ For getting $V_{c(min)}$ equating (4) & (5).

$$\Rightarrow \quad \alpha V_s - (1-\alpha)V_c = \left[\alpha V_s + (1-\alpha)V_c\right] \frac{R_L}{R_L+R_3}$$

$$\alpha V_s - (1-\alpha)V_c = \alpha V_s \cdot \frac{R_L}{R_L+R_3} + (1-\alpha)V_c \cdot \frac{R_L}{R_L+R_3}$$

$$\alpha V_s - \alpha V_s \left[\frac{R_L}{R_L+R_3}\right] = (1-\alpha)V_c + (1-\alpha)V_c \left[\frac{R_L}{R_L+R_3}\right]$$

$$\alpha V_s \left[1 - \frac{R_L}{R_L+R_3}\right] = (1-\alpha)V_c \left[1 + \frac{R_L}{R_L+R_3}\right]$$

$$\alpha V_s \left[\frac{R_L+R_3-R_L}{R_L+R_3}\right] = (1-\alpha)V_c \left[\frac{R_L+R_3+R_L}{R_L+R_3}\right]$$

$$\alpha V_s \left[\frac{R_3}{R_L+R_3}\right] = (1-\alpha)V_c \left[\frac{R_3+2R_L}{R_L+R_3}\right]$$

$$\frac{\alpha V_s R_3}{(R_L+R_3)} = \frac{(1-\alpha)V_c\,[R_3+2R_L]}{(R_L+R_3)}$$

$$\alpha V_s R_3 = (1-\alpha)V_c\,[R_3+2R_L]$$

$$V_c = \frac{\alpha}{1-\alpha} \cdot \frac{R_3}{R_3+2R_L} \cdot V_s$$

$$V_c = \frac{\frac{R_2}{R_1+R_2}}{\frac{R_1}{R_1+R_2}} \cdot \frac{R_3}{R_3+2R_L} \cdot V_s$$

$$V_c = \frac{R_2}{R_1} \cdot \frac{R_3}{R_3+2R_L} \cdot V_s$$

$$\boxed{V_{c(min)} = \frac{R_2}{R_1} \cdot \frac{R_3}{R_3+2R_L} \cdot V_s}$$

$V_{c(min)}$ value depends upon the load resistor R_L.

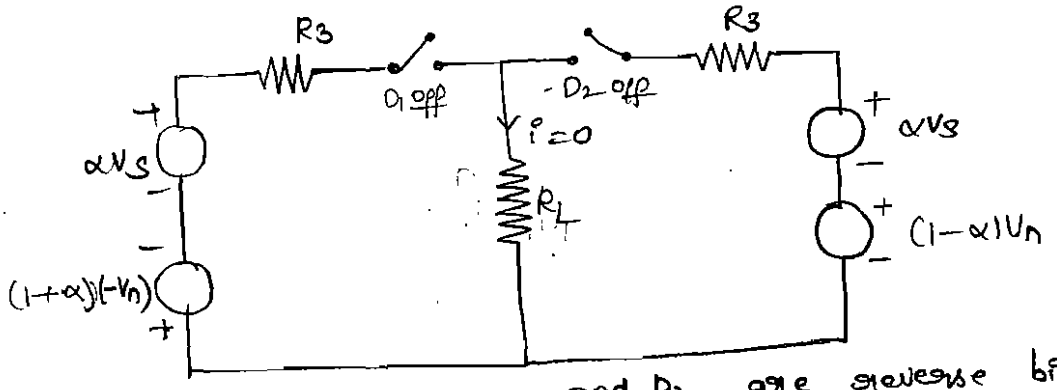
→ By varying the R_L value then $V_{c(min)}$ value get varied.

(ii) Minimum control voltage $V_{n(min)}$ to ensure that D_1 and D_2 are reverse biased :—

→ A minimum Control voltage $V_{n(min)}$ is required to keep the diodes off when no sampling takes place.

→ When both the diodes are reverse biased, the point P is at ground potential. which is the output value. It is shown in below figure

→ As D_1 is reverse-biased, it behaves as an open circuit, as a result the input appears at the output.



→ Equalent Circuit when D_1 and D_2 are reverse biased

Apply KVL in the second loop

V_{D2} = voltage across D_2 = $\alpha V_s + (1-\alpha)V_n = V_{D2}$

→ Here we consider the magnetude of control signal as V_n, so V_c is replaced by V_n in the above equation

then $V_{D2} = \alpha V_s + (1-\alpha) V_n$.

→ For calculating $V_{n(min)}$, the diodes will be reverse biased, then voltage across the diodes will be zero. then no current will be passing through the load resistor R_L so we take V_{D2} as 0.

→ so equating the above equation to zero

then

$$\Rightarrow \alpha V_s + (1-\alpha) V_n = 0.$$

$$(1-\alpha) V_n = -\alpha V_s.$$

$$V_n = -\frac{\alpha V_s}{1-\alpha}.$$

$$V_n = -\frac{R_2}{R_1} V_s.$$

$$\boxed{V_{n(min)} = -\frac{R_2}{R_1} V_s.}$$

$$\left[\because \frac{\alpha}{1-\alpha} = \frac{\frac{R_2}{R_1+R_2}}{\frac{R_1}{R_1+R_2}} \quad \frac{\alpha}{1-\alpha} = \frac{R_2}{R_1}\right]$$

→ Disadvantages of two diode bidirectional Sampling gates:—

i) Its gain is low

ii) It is sensitive to control voltage imbalance

iii) There is a possibility that $(V_n)_{min}$ may be excessive

iv) There may be appreciable leakage through the diode capacitance.

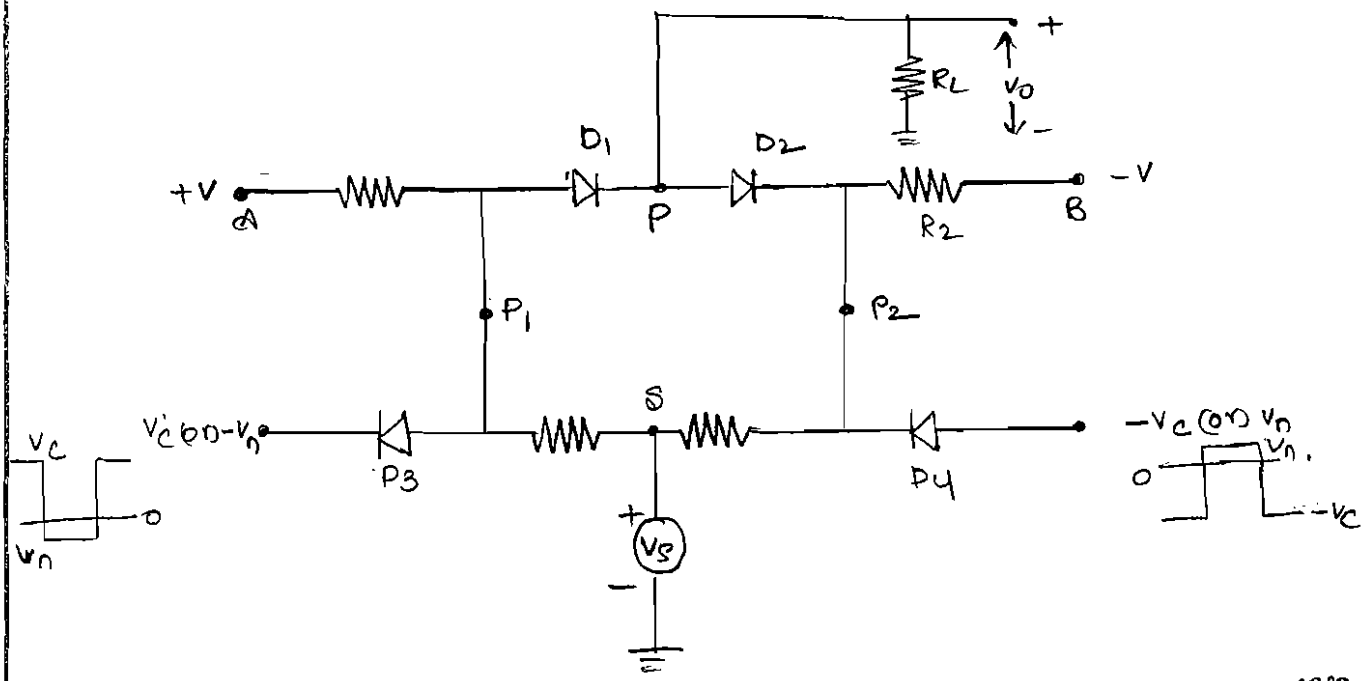
→ Four diode Sampling gate :—

→ To overcome the disadvantages of two diode sampling gate, a four diode sampling gate will be designed.

→ This is obtained by adding two more diodes to the two diode Sampling gate.

→ Two balanced voltages +V and −V also required.

→ The circuit is shown in below.



→ The control signals are connected through the two additional diodes D_3 and D_4 to points P_1 and P_2

→ When the control voltages are V_c & $-V_c$ are applied, then the diodes D_3 and D_4 are reverse biased, and are off.

→ Because of the +V and −V voltages, the diodes D_1 & D_2 will be ON.

→ Then input signal is transmitted to the load through a Resistor R_1.

→ And the control signals are at $-V_n$ and V_n are applied then D_3 & D_4 will be conduct.

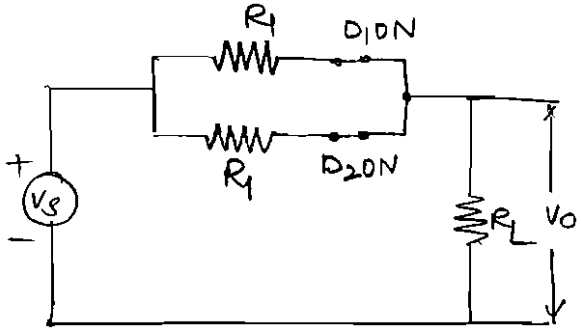
→ As a result D_1 & D_2 are off and now the output is zero.

→ when D_3 & D_4 are off, the circuit is similar to the two diode gate. during transmission except that the voltage V_c & $-V_c$ are replaced by $+V$ & $-V$ respectively

→ hence the gain of this circuit is same as two diode bi-directional sampling gate.

$$\text{i.e } A = \frac{R_2}{R_1+R_2} \cdot \frac{R_L}{R_L+R_3/2} \cdot V_0$$

→ when D_1, D_2 are ON & D_3, D_4 are off, the circuit is looks like as.



→ In previously we have to derive that $V_{c\min}$, four diode gate has also the same value

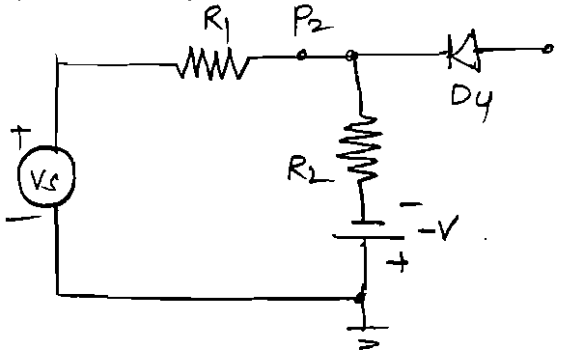
→ so from two diode sampling gate

$$V_{min} = \frac{R_2}{R_1} \times \frac{R_3}{R_3+2R_L} V_S$$

→ let us now we compute $V_{c\min}$. If $R_f \ll R_L$ for a positive V_s the voltage at P1 is AV_s, if D_3 is to be off. then V_c must atleast equal to AV_s

$$\text{i.e } V_{c\min} \geq AV_s$$

→ $V_{n(min)}$ is calculated to satisfy that condition is D_2 is off & D_4 is ON. then we calculate the voltage at the cathode of D_4 due to sources $-V$ and V_s.



By using Superposition theorem

$$V_n(min) = V_s \times \frac{R_2}{R_1+R_2} - V \times \frac{R_1}{R_1+R_2}$$

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